INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2007 EDITION

EXECUTIVE SUMMARY

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ACKNOWLEDGMENTS

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We acknowledge and thank the regional teams for their support:

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INTRODUCTION

OVERVIEW

For more than four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor throughput**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last three decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments, and other research providers or funders. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS is a dynamic process, evident by the evolution of the ITRS documents. The ITRS reflects the semiconductor industry migration from geometrical scaling to equivalent scaling. Geometrical scaling [such as Moore's Law] has guided targets for the previous 30 years, and will continue in many aspects of chip manufacture. Equivalent scaling targets, such as improving performance through innovative design, software solutions, and innovative processing, will increasingly guide the semiconductor industry in this and the subsequent decade. Since 2001 the ITRS has responded by introducing new chapters on System Drivers (2001), Emerging Research Devices and Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (2005), and most recently in 2007, Emerging Research Materials, to better reflect this evolution of the semiconductor industry.

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of electronics would further reduce the cost per function (historically, ~25–29%% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?"

It is forecasted that by the end of the next decade it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices that will hopefully realize some properties beyond the ones of CMOS devices. However, it is believed that most likely these new devices will not have all the properties of CMOS devices and therefore it is anticipated that heterogeneous integration either at the chip level or at the package level will integrate these new capabilities around a CMOS core.

The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensures that the 2007 ITRS remains the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The complete 2007 ITRS and past editions of the ITRS are available for viewing and printing as electronic documents at the Internet web site *http://www.itrs.net*.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each sponsoring region (Europe, Japan, Korea, Taiwan, and the U.S.A.). The principal IRC functions include the following:

- Providing guidance/coordination for the International Technology Working Groups (ITWGs)
- Hosting the ITRS Workshops
- Editing the ITRS

The International Technology Working Groups write the corresponding technology-area chapters of the ITRS. The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the 2007 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- Process Integration, Devices, and Structures
- RF and Analog / Mixed-signal Technologies for Wireless Communications
- Emerging Research Devices
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging

Crosscut ITWGs are the following:

- Emerging Research Materials
- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

The ITWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. The demographics per ITWG reflect the affiliations that populate the technology domains. For example, with a longer-term focus area such as Emerging Research Devices, the percentage of research participants is higher than suppliers. In the process technologies of Front End Processes, Lithography, and Interconnect, the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.

For the 2007 edition, three ITRS meetings were held worldwide as follows: Annecy, France (sponsored by the ESIA and hosted by STMicroelectronics); San Francisco, U.S.A., sponsored by the SIA, organized by SEMATECH and co-hosted with SEMI/North America; and Chiba, Japan (sponsored and co-hosted by JEITA and SEMI Japan). These meetings provided the main forums for face-to-face discussions among the members of each ITWG and coordination among the

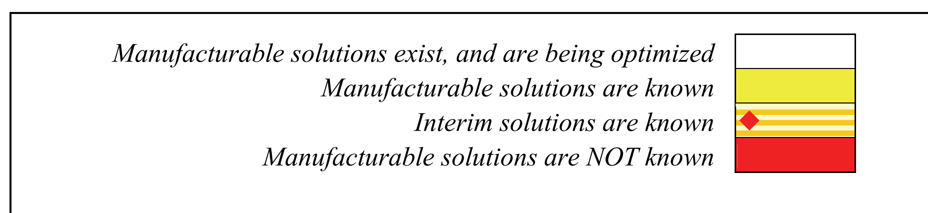
different ITWGs. In addition, the ITRS teams hold public ITRS conferences bi-annually to present the latest Roadmap information and to solicit feedback from the semiconductor industry at-large.

The ITRS is released annually, with updates and corrections to data tables each even-numbered year (such as 2000, 2002, 2004, 2006) while complete editions are released each odd-numbered year (2001, 2003, 2005, 2007). This ITRS process thus ensures continual assessment of the semiconductor industry's near and long-term needs. It also allows the teams to correlate in a timely fashion the ITRS projections to most recent research and development breakthroughs that may provide solutions to those needs.

ROADMAP CONTENT

The ITRS assesses the principal technology needs to guide the shared research, showing the "targets" that need to be met. These targets are as much as possible quantified and expressed in tables, showing the evolution of key parameters over time. Accompanying text explains and clarifies the numbers contained in the tables where appropriate.

The ITRS further distinguishes between different maturity or confidence levels, represented by colors in the tables, for these targets:



The first situation, "Manufacturable solutions exist, and are being optimized," indicates that the target is achievable with the currently available technology and tools, at production-worthy cost and performance. The yellow color is used when additional development is needed to achieve that target. However, the solution is already identified and experts are confident that it will demonstrate the required capabilities in time for production start. The situation "Interim Solutions are Known" means that limitations of available solutions will not delay the start of production, but work-arounds will be initially employed in these cases. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity. The fourth and last situation is highlighted as "red" on the Roadmap technology requirements tables and has been referred to as the "Red Brick Wall" since the beginning of ITRS. (The "red" is officially on the Roadmap to clearly warn where progress might end if tangible breakthroughs are not achieved in the future.) Numbers in the red regime, therefore, are only meant as warnings and should not be interpreted as "targets" on the Roadmap. For some Roadmap readers, the "red" designation may not have adequately served its *sole* purpose of highlighting significant and exciting challenges. There can be a tendency to view *any* number in the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

"Red" indicates where there are no "known manufacturable solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. An analysis of "red" usage might classify the "red" parameters into two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry doesn't have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end)

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (manufacturable solutions are known) and, ultimately "white" (manufacturable solutions are known and are being optimized) in future editions of ITRS.

As indicated in the overview, the Roadmap has been put together in the spirit of defining what technical capabilities the industry needs to develop in order to stay on Moore's Law and the other trends, and when. So the ITRS is not so much a forecasting exercise as a way to indicate where research should focus to continue Moore's law. In that initial "challenge" spirit, the Overall Roadmap Technology Characteristics (ORTC) team updates key high-level technology needs, which establish some common reference points to maintain consistency among the chapters. The high-level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies.

Over the years, however, the Roadmap has sometimes been seen as a self-fulfilling prophecy. To a certain extent this is also a valid view, as companies have benchmarked each other against the Roadmap, and it proved very effective in providing thrust for research. So it is not unreasonable to use the Roadmap targets, when manufacturing solutions or acceptable workarounds are known, as guidelines to forecasting exercises.

What these targets should never be used for, however, is as basis for legal claims in commercial disputes or other circumstances. In particular, the participation in the ITRS roadmapping process does not imply in any way a commitment by any of the participating companies to comply with the Roadmap targets. We recall that the ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual product or equipment.

TECHNOLOGY CHARACTERISTICS

As mentioned above, a central part of the IRC guidance and coordination is provided through the initial creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics (ORTC) tables. Each ITWG chapter contains several principal tables. They are individual ITWGs' technology requirements tables patterned after the ORTC tables. For the 2007 ITRS, the ORTC and technology requirements tables are fully annualized and in both the "Near-term Years" (2005, 2006… through 2015) and "Long-term Years" (2016, 2017 … through 2022) This format is illustrated in Table B, which contains a few key rows from lithography-related ORTC Table 1a and 1b, including the new Flash product uncontacted polysilicon half-pitch technology trend line item. In the previous 2005 Roadmap editions, the DRAM stagger-contacted M1 half pitch line item was used as a standard header for all the ITRS ITWG tables; however, beginning with the 2007 edition, the IRC has requested that only the year of first production be required as a standard header. At the discretion of the ITWGs, other product technology trend driver line items may be selected from ORTC Table 1a and 1b for use in their ITWG tables as overall headers indicating key drivers for their tables.

Table B ITRS Table Structure—Key Lithography-related Characteristics by Product

Near-term Years

YEAR OF PRODUCTION	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	**65**	**57**	**50**	**45**	**40**	**36**	**32**	**28**	**25**
MPU/ASIC stagger-contacted Metal 1 (M1)½ Pitch (nm)	**68**	**59**	**52**	**45**	**40**	**36**	**32**	**28**	**25**
Flash Uncontacted Poly Si ½ Pitch (nm)	**54**	**45**	**40**	**36**	**32**	**28**	**25**	**23**	**20**
MPU Printed Gate Length (nm)	**42**	**38**	**34**	**30**	**27**	**24**	**21**	**19**	**17**
MPU Physical Gate Length (nm)	**25**	**23**	**20**	**18**	**16**	**14**	**13**	**11**	**10**

Long-term Years

YEAR OF PRODUCTION	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	**22**	**20**	**18**	**16**	**14**	**13**	**11**
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	**22**	**20**	**18**	**16**	**14**	**13**	**11**
Flash Uncontacted Poly Si ½ Pitch (nm)	**18**	**16**	**14**	**13**	**11**	**10**	**9**
MPU Printed Gate Length (nm)	**15**	**13**	**12**	**11**	**9**	**8.4**	**7.5**
MPU Physical Gate Length (nm)	**9**	**8**	**7**	**6.3**	**5.6**	**5.0**	**4.5**

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. Please refer to the Glossary *for detailed definitions for Year of Introduction and Year of Production.*

TECHNOLOGY PACING

In previous editions of the ITRS, the term "technology node" (or "hpXX node") was used in an attempt to provide a single, simple indicator of overall industry progress in integrated circuit (IC) feature scaling. It was specifically defined as the smallest half-pitch of contacted metal lines on any product. Historically, DRAM has been the product which, at a given time, exhibited the tightest contacted metal pitch and, thus, it "set the pace" for the ITRS technology nodes. However, we are now in an era in which there are multiple significant drivers of scaling and believe that it would be misleading to continue with a single highlighted driver, including DRAM

For example, along with half-pitch advancements, design factors have also rapidly advanced in Flash memory cell design, enabling additional acceleration of functional density. Flash technology has also advanced the application of electrical doubling of density of bits, enabling increased functional density independent of lithography half-pitch drivers. A second example is given by the MPU/ASIC products, for which the speed performance driver continues to be the gate-length isolated feature size, which requires the use of leading-edge lithography and also additional etch technology to create the final physical dimension.

Significant confusion relative to the historical ITRS node definition continues to be an issue in many press releases and other documents that have referred to "node acceleration" based on other, frequently undefined, criteria. Of course, we now expect different IC parameters to scale at different rates, and it is certainly legitimate to recognize that many of these have product-specific implications. In the 2007 ITRS, we will continue the practice of eliminating references to the term "technology node." As mentioned above, the IRC has recommended that the only standard header will be year of first production, and DRAM M1 half-pitch is just one among several historical indicators of IC scaling. With this latest change to standard ITRS table format policy, it is hoped that the ITRS will not contribute to industry confusion related to the concept of "technology node." Of course, "node" terminology will continue to be used by others. Hopefully, they will define their usage within the context of the application to the technology of a specific product.

For reference on the 2005 ITRS common definition of M1 half-pitch for all products, as well as the definition of polysilicon half-pitch for FLASH memory, see Figure 1.

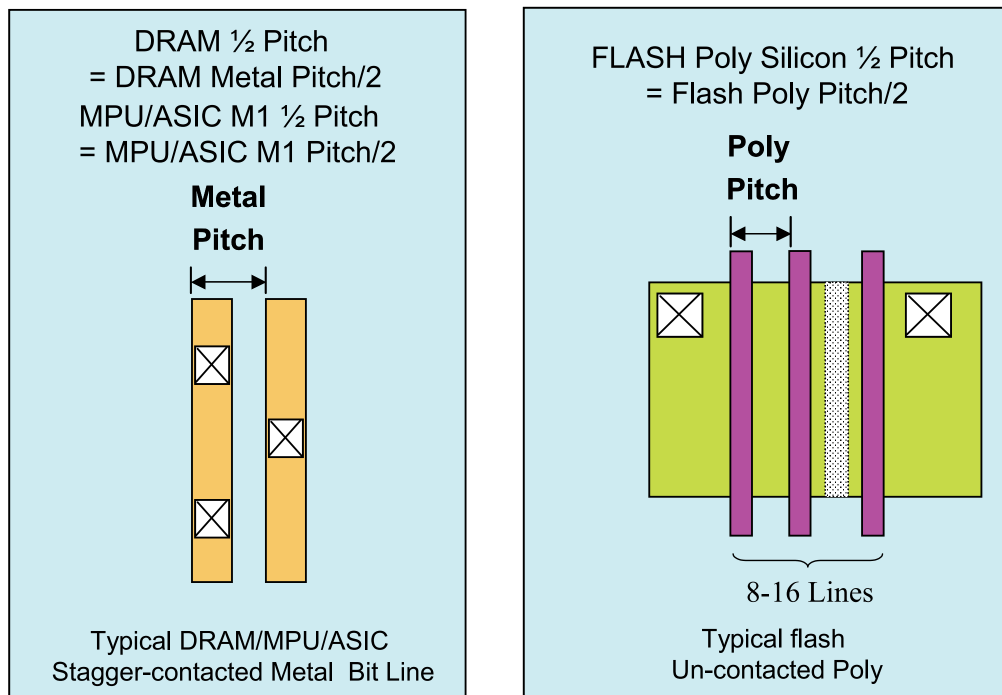


Figure 1 2005 Definition of Pitches

MEANING OF ITRS TIME OF INTRODUCTION

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the ITRS is the "Year of Production," which is defined in Figure 2.

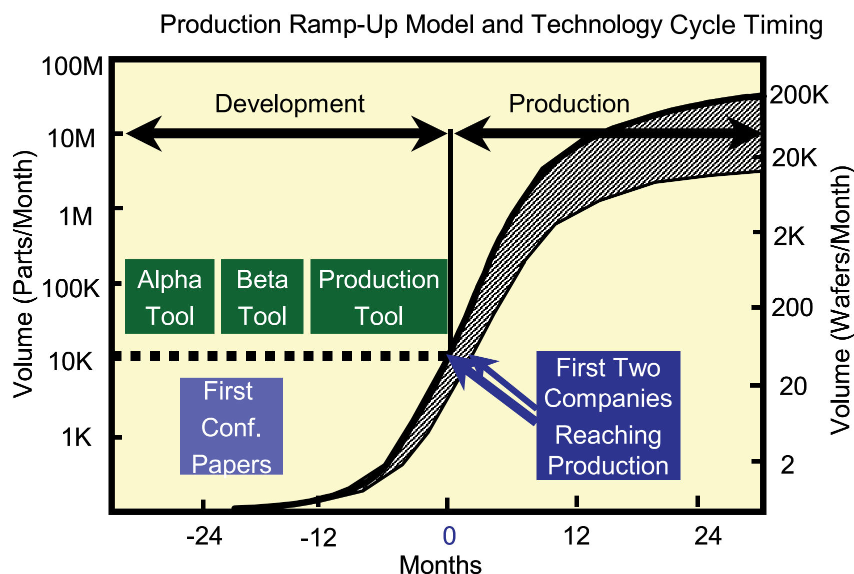


Figure 2 A Typical Production "Ramp" Curve

The "Production" time in the ITRS refers to the time when the first company brings a technology to production and a second company follows, typically within three months. Production means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero (0)" in Figure 2 can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity or more, the time to ramp from 20 WSPM to full capacity can take nine to twelve months. This time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month if the chip size were 140 mm^2 (430 gross die per 300 mm wafer × 20K WSPM × 70% total yield from wafer starts to finished product = 6M units/month).

In addition, note that the ITRS ramp timing in this example is in reference to the ramp of a technology cycle within a given wafer generation. Now that the time for a new wafer generation transition, 450mm, is nearly upon us, additional scrutiny must be given to the historical ramp rate for a technology cycle that may be ramped in two wafer generations of the first leading companies at the same time. It is during that transition of a technology cycle coexisting within two wafer generations that the economic productivity gain modeling is also examined.

2007 SICAS Industry Manufacturing Technology Capacity Update

It is noted that the ITRS, by its definition, focuses on forecasting the earliest introduction of the leading-edge semiconductor manufacturing technologies, which support the production of selective leading-edge driver product markets, such as DRAM, Flash, MPU, and high-performance ASICs. It is, however, true that many companies, for a variety of reasons, may choose to introduce a leading-edge technology later than the earliest introduction of the leading-edge technology; hence, there is a wide variation of the technologies in actual production status from leading edge to trailing edge.

Figure 3 shows, in horizontal bar graph format (each bar width is proportional to silicon processing capacity), the actual, annual worldwide wafer production technology capacity distributions over different process feature sizes. The distributions of the overall industry technology capacity segments are tracked by feature-size splits, which are quite widespread.

The ITRS technology cycle, as measured by DRAM metal 1 (M1) half-pitch, is shown as yellow marks (for the historical actual timing), as reported by the industry surveys conducted by ITRS TWGs. The surveys conducted in 2003, 2005, and 2007 have indicated that first production of the leading-edge DRAM M1 half-pitch has been on a two-year cycle (for 0.71× reduction), from 250 nm in 1998 through 90 nm in 2004. However, the most recent survey update is indicating that the DRAM historical trend is tracking closer to the ITRS MPU trend. This will be investigated further in 2007 and reported in the 2008 Update. Details are included in the 2007 PIDS chapter.

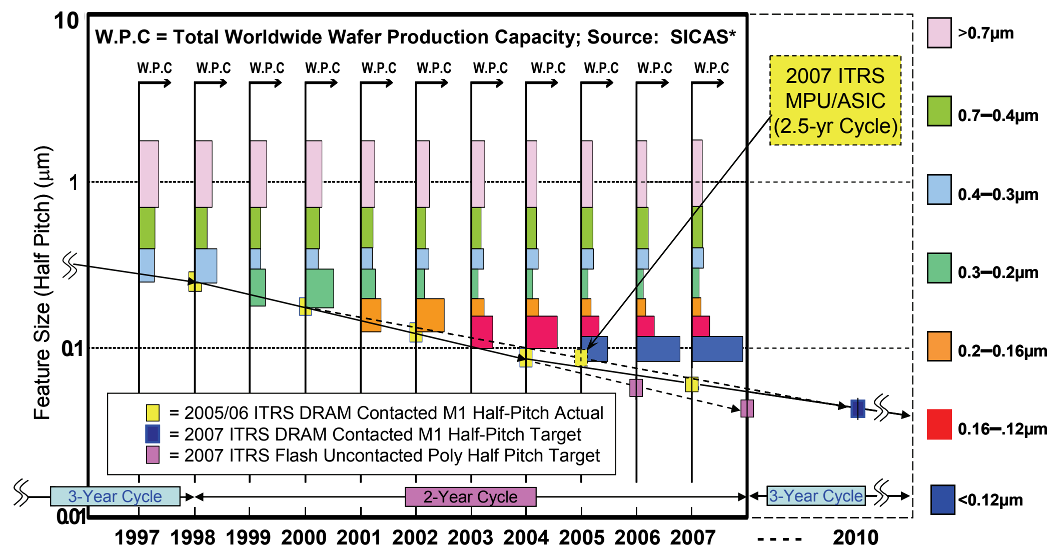
The blue mark indicates the timing for the next 2007 ITRS target for the 45 nm technology in 2010. Subsequent targets for 0.71× reduction of the DRAM M1 half-pitch are placed on a three-year cycle through the present ITRS roadmap horizon in 2022. Also included is the tracking of the Flash technology capacity trend for uncontacted poly; which has grown rapidly in market demand, and now contributes significantly to the industry capacity.

Note that the first production of the leading-edge feature size has historically ramped into a 20–30% industry capacity share within one year, and the timing of that 20–30% capacity share has been on the same cycle as the timing for first production. Furthermore, the relative percentage of the most leading-edge technology capacity has been rapidly growing. The combined capacity of the most recent two technology generations has typically grown to nearly half the capacity of the industry within two to three years after their introduction. The 2007 ITRS has updated the Flash technology trend to continue on a two-year cycle until 2008, which should add even more capacity at the most leading edge.

It should be noted that the capacity for the most leading edge technology (65 nm) is presently only available within the SICAS “<0.12” capacity split. The availability of the “<0.08 µ” split survey data, which would include the rapidly ramping 65 nm Flash technology cycle capacity, has been delayed from SICAS until late in 2007, therefore the actual analysis of the two-year or three-year technology demand cycle (to 20–30% of total MOS capacity) will not be available until the 2008 Update of the ITRS.

It is also notable that relative share of trailing edge capacity continues to appear to not decline as rapidly as might be expected (migrate upward to leading-edge); and the leading-edge capacity split shares should be expected to continue to “crowd” as products migrate to the most leading-edge capacity (“<0.08 µ” capacity data, when available). This phenomenon continues to hold significant implication for the markets and business models of the materials and equipment suppliers that ultimately develop and deliver the required solutions to the ITRS technology “Grand Challenges.”

Suppliers must support not only longer-lasting trailing edge factories, but also many diverse technology factories at the leading edge. In addition, suppliers must deliver alpha and beta tools and materials two to three years ahead of the first production requirement, and then they must be prepared to ramp into production with overlapping technology demand capacities. These scenarios present both a market opportunity and also an R&D and support resource challenge to both suppliers and manufacturers, especially with the looming probability of 450 mm wafer generation investments.



Note: The wafer production capacity data are plotted from the Semiconductor Industry Association (SIA) Semiconductor Industry Capacity Statistics (SICAS) 4Q data for each year, except 2Q data for 2007. The width of each of the production capacity bar corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.

Figure 3 Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution[1]

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[1] *The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS*

ROADMAP SCOPE

Traditionally, the ITRS has focused on the continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, since 2001, we have reached the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths below 9 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the ITRS must address post-CMOS devices. The Roadmap is necessarily more diverse for these devices, ranging from more familiar non-planar CMOS devices to exotic new devices such as spintronics. Whether extensions of CMOS or radical new approaches, post-CMOS technologies must further reduce the cost-per-function and increase the performance of integrated circuits. In addition, product performance increasingly does not scale only with the number of devices, but also with a complex set of parameters given by design choices and technology. Thus new technologies may involve not only new devices, but also new manufacturing and design paradigms.

Microprocessors, memories, and logic devices require silicon-based CMOS technologies. The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. The essential functions on such a system-on-chip (SoC) are data storage and digital signal processing. However, many quantitative requirements, such as power consumption and communications bandwidth (e.g., RF), and many functional requirements, such as the functions performed by passive component, sensors and actuators, biological functions, and even embedded software functions, do not scale with Moore’s Law. In many of these cases, non-CMOS solutions are employed. In the future, the integration of CMOS- and non-CMOS based technologies within a single package (or system-in-package, (SiP)) will become increasingly important. In terms of functionality, SoC and SiP can be complementary, and hence are not necessarily competing with each other. Functions initially fulfilled by non-CMOS dedicated technologies may eventually be integrated onto a CMOS SoC, using mixed technologies derived from core CMOS. Consequently, the partitioning of system-level functions between *and within* SoC and SiP is likely to be dynamic over time. This will require innovations in cross-disciplinary fields, such as nano-electronics, nano-thermomechanics, nano-biology, extremely parallel software, etc. For SiP applications, packaging will be a functional element and a key differentiator. This trend is represented graphically in Figure 4.

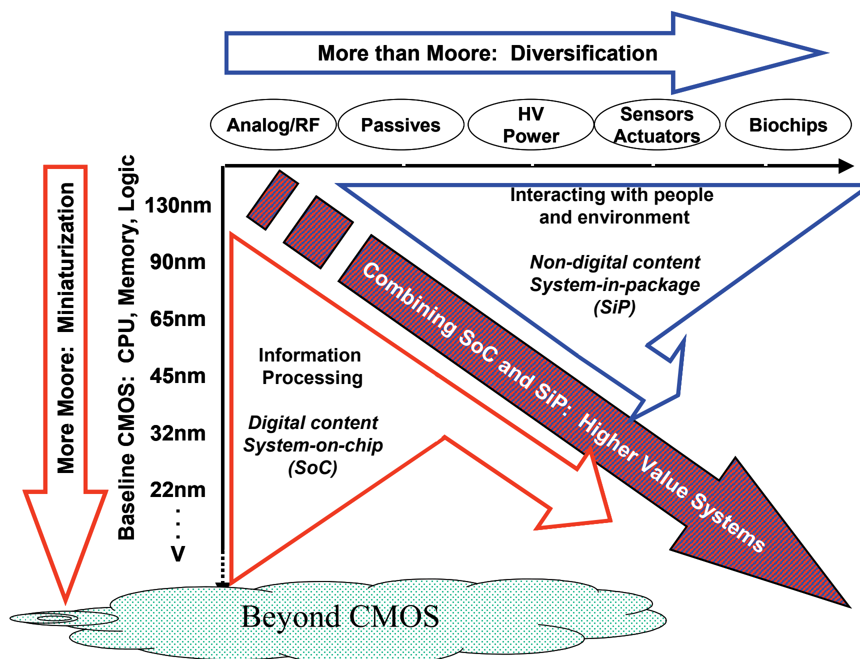

Figure 4 Moore’s Law and More

Capacity) and published by the Semiconductor Industry Association (SIA), as of August, 2007. The detailed data are available to the public online at the SIA website, http://www.sia-online.org/pre_stat.cfm .

This concept of "More than Moore," introduced in the 2005 roadmap, has been further discussed and refined for the 2007 edition of the roadmap. In particular, a consensus has been reached on the following definitions. (Refer to Figure 4):

1. Scaling ("More Moore," vertical axis)

    1a. *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.

    1b. *Equivalent Scaling* which occurs in conjunction with, and also enables, continued Geometrical Scaling, refers to (a) 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the performance of the chip; (b) novel design techniques and technology such as multi-core design. The objective of Equivalent Scaling is the continuation of "Moore's Law."

2. Functional Diversification ("More than Moore", horizontal axis)

Functional Diversification refers to the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board level into a particular package-level (SiP) or chip-level (SoC) implementation. In addition, the increasingly intimate integration of complex embedded software into SoCs and SiPs means that software might also need to become a fabric under consideration that directly affects performance scaling. The objective of "More than Moore" is to incorporate digital and non-digital functionality into compact systems.

It is expected that the relative weight of the "More than Moore" component of the industry evolution will increase over time. This increase leads to a growing diversity of the scientific fields that the research must cover in order to sustain the pace of innovation, while the financial constraints are becoming tighter. The question of the guidance of the research efforts, in which the ITRS is playing a pivotal role, is therefore crucial. Taking this into consideration, various working groups of the ITRS have been investigating the consequences of the "More than Moore" trend in their field of expertise. The results of that work, which will further gain momentum in the coming years, can be found in their respective chapters.

The scope of the 2007 ITRS specifically includes detailed technology requirements for all CMOS integrated circuits, including wireless communication and computing products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to design and manufacture CMOS ICs are also used for other products such as compound semiconductor, discrete, optical, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most IC-technology-based micro/nanotechnologies, even though that is not the explicit purpose of the Roadmap.

2007 ITRS SPECIAL TOPICS

EMERGING RESEARCH MATERIALS

Many of the new device and memory concepts that are being discussed in the ERD chapter will employ new materials, for example, for the device itself as well as for interconnect and passivation. The requirements for these new materials are critically dependant on the properties and specifications of the new devices and memories. This led in 2005 to the creation, within the ERD chapter, of a sub-group for Emerging Research Materials (ERM). In this edition of the roadmap, this subgroup has now become a full-fledged working group, and the results of this work are published in a dedicated Emerging Research Materials (ERM) chapter.

TRANSITION TO 450 MM

In the 2005 edition of the Roadmap, 2012 was adopted as the year of introduction of 450 mm wafers in volume production. This date of introduction depends not only on the mastering of all technical issues, associated with the transition of 450 mm, but also on the preparedness of the industry. Accordingly, during the past two years, the ITRS working groups and the IRC have been further collecting data to evaluate the timing of the introduction of 450 mm in production.

The rationale for a transition to 450 mm diameter wafer is productivity, one of the enablers of Moore's law. This is the ability—everything else staying the same—to decrease the manufacturing cost of each mm² of IC by the use of larger diameter wafers. Based on economic considerations, the International SEMATECH Manufacturing Initiative (ISMI) () has determined that to stay on this productivity curve, the industry needs to achieve 30% cost reduction and 50% cycle time improvement in manufacturing by 2012, which in their opinion is achievable only via a transition to 450 mm (while

the cost reduction goal has been achieved through previous wafer generation changes, the cycle time goal is new). This opinion was reinforced by the conclusions of an analysis of potential 300 mm improvements, which showed that the so-called "300 mm Prime" program has cycle time opportunity but falls short of the traditional cost reduction required to stay on Moore's Law. This realization prompted ISMI to kick-off the 450 mm initiative in July 2007.

There are, however, several arguments to question this 2012 timing:

- On the equipment suppliers' side, having production equipments available in 2012 means that alpha tools must be available by 2009. So far no key suppliers have announced plans for a prototype tool by 2012.
- On the manufacturers' side, an important question is related to the initial investment "step function": the promises for productivity gains in 300 mm Fabs have proved to become true for very large investments, in the range of $4B or beyond. One might expect that the minimal economical size of a 450 mm Fab will be even larger, putting it beyond the reach of many companies. Furthermore, while an economic model which takes into consideration the industry as a whole may conclude that 2012 is the right time for transition to 450 mm, decision of individual companies may differ. So both the initial rate of growth of the 450 mm equipment market and its size at maturity can be questioned, which could lead equipment suppliers to delay their investment in the development of this new generation.
- Finally, readiness of wafer manufacturers is unclear: The Front-End Processes working group is now estimating that wafer suppliers will move the work on 450 mm wafers from research to development in 2009. For 300 mm, this transition occurred approximately seven years before 300 mm was used by IC manufacturers in production. So this would indicate a transition date for IC manufacturers to start moving to 450 mm in 2016.

Given all of the above, the ITRS is proposing a target range of 2012 to 2016 for the introduction of 450 mm wafers in production.

GRAND CHALLENGES

IN THE NEAR-TERM (THROUGH 2015) AND LONG-TERM (2016 AND BEYOND)

OVERVIEW

The continued research and development efforts in our industry have brought about reacceleration and diversification of scaling. Flash device's scaling continues a two-year cycle until 2008, MPU is a 2.5-year cycle until 2010, and DRAM is a three-year cycle. The word "node" cannot define technology trend clearly anymore. In the chapter on PIDS, it is observed that there are many choices to improve MOSFET performance, which we call "Parallel Paths" of planer bulk metal-oxide semiconductor field effect transistor (MOSFET), fully depleted, silicon-on-insulator (FD-SOI) MOSFET, and multiple gate [e.g., field effect transistor structures (Fin-FET)]. The ITRS is entering a new era as the industry begins to address the theoretical limits of CMOS scaling. There remain many technological challenges in patterning, advanced materials, strain engineering particularly in non-planar device structures, junction leakage, process control, and manufacturability. Challenges also span SoC and SiP integration of CMOS with new types of memory devices. All these will be essential elements for the continuous growth of the semiconductor industry.

Each ITWG identified and listed "Difficult Challenges", which are included in this Executive Summary. In this section of "Grand Challenges," major "Difficult Challenges" are selected and described. This section is intended to help readers grasp an overall picture concerning major technological issues.

These "Grand Challenges" are classified into two categories: "Enhancing Performance" and "Cost-effective Manufacturing." They are also described according to the "near term" (2007 through 2015) and the "long term" (2016 through 2022) timeframes of the Roadmap.

IN THE NEAR TERM (THROUGH ~ 2015)

ENHANCING PERFORMANCE

LOGIC DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, FRONT END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

Scaling planar CMOS will face significant challenges. The conventional path of scaling, which was accomplished by reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping, might no longer meet the application requirements set by performance and power consumption. Introduction of new material systems as well as new device architecture, in addition to continuous process control improvement are needed to break the scaling barriers.

Reduction of the equivalent gate oxide thickness (EOT) has emerged as the most difficult challenge associated with the future device scaling, which is required for performance improvement. For low-power (LP) applications, oxynitride will no longer meet the strict leakage current requirement. For high-performance (HP) applications, EOT of less than 1 nm with adequate reliability is needed. Therefore, introduction of higher dielectric constant (high-κ) material in which tunneling current can be suppressed without sacrificing current drive will be necessary. The complete gate stack material systems need to be optimized together for best device characteristics and cost. These material changes pose a great challenge in MOSFET technology, where silicon dioxide/poly Si has long played a central role as the most reliable gate stack system.

Planar MOSFET requires high-channel doping to control short-channel effects, the trade-offs are mobility degradation and increased leakage power consumption. Using doping to control threshold voltage in scaled device also causes increasing variation of the threshold voltage, posing difficulty in circuit design while scaling the supply voltage. New device architecture such as ultra-thin body, FD-SOI, and multiple-gate MOSFETs (e.g., finFETs) are expected. A particularly challenging issue is the control of the thickness, including its variability, of these ultra-thin MOSFETs. The solutions for these issues should be pursued concurrently with circuit design and system architecture improvements.

MEMORY DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FRONT-END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

The continued research and development efforts in the industry have brought about reacceleration and diversification of scaling. The baseline memories now includes both stand-alone and embedded DRAM, SRAM, and both NAND and NOR Flash. The new prototype memories table includes silicon/oxide/nitride/oxide/silicon (SONOS), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase-change memory (PCM).

The challenges for DRAM devices are adequate storage capacitance with reduced feature size, high-κ dielectrics implementation, low leakage access device design, and low sheet resistance materials for bit and word lines. For stand-alone DRAM, high-κ materials are currently being used in an SIS structure for trench capacitors. Metal top electrode will be needed by 2007 and a full MIM structure with high-κ dielectric may be needed by 2009, when a dielectric constant greater than 60 is required for beyond 50 nm. Embedded DRAM in SOC applications will drive additional integration challenges. One such key challenge is the matching between the ground rules required for the deep contacts around the stacked capacitor with the contact ground rules for the logic devices.

The need for advanced capacitor materials in trench DRAM are postponed relatively to the stacked capacitor by a few years; however the cell size factor for stack capacitor DRAM is 6, while that for the trench DRAM remains at 8. Novel cell concepts for the trench capacitor, depending upon the replacement of the conventional planar transfer device by 3D array transistor structures, are envisaged for 65 nm in order to alleviate device scaling issues.

The rapid expansion of the market for Flash memories brings more focus on the material and process challenges for these devices. With this acceleration, Flash memory is becoming a new technology driver for both critical dimension scaling and material technology. The effective dimension, F, of Flash NAND device now appears to lead the DRAM half pitch.

The key challenges in Flash memory device are non-scalability of tunnel dielectrics, non-scalability of interpoly dielectrics, dielectric material properties, and dimensional control. In Flash memory devices, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. It is no longer feasible for the control gate poly Si to overlap the sides of the floating gate as the space between adjacent poly Si gates shrink. Thus, by 2010 high-κ interlayer dielectrics will be required to maintain an acceptable coupling ratio. Flash memory challenges also include the inception into mainstream manufacturing and the scaling of new memory types and storage concepts such as MRAM, phase-change memory, and FeRAM, for example. MRAM scalability of cell-size and write-power reduction needs solutions as early as 2008. FeRAM critical issues relate to cell endurance, scalability of power supply and cell-size.

HIGH-PERFORMANCE, LOW-COST RF AND ANALOG/MIXED-SIGNAL SOLUTIONS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS]

Fundamental changes in materials and device structures will be required to sustain continued performance, power management, and density improvements. The introduction of new materials such as high-permittivity (high-κ) gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes poses clear challenges to attain equivalent levels of threshold voltage, current mismatch, and for 1/f noise. The electrical characteristics of non-classical CMOS, such as dual-gate, fully depleted SOI devices, are fundamentally different from that of conventional CMOS. Thus, the fabrication of conventional precision analog/RF driver devices, resistors, and varactors may require separate process steps with the attendant increase in die cost. Furthermore, the steady reduction in analog supply voltage poses a significant circuit design challenge.

Signal isolation, especially between the digital and analog regions of the chip, is another important challenge for scaled technologies and for increased integration complexity. Noise coupling may occur through the power supply, ground, and shared substrate. The difficulty of integrating analog and high-performance digital functions on a chip increases with scaling in both device geometry and supply voltage. Signal isolation is critical for success in co-integrating high-performance analog circuits and highly complex digital signal processing (DSP) functions on the same die or substrate. Such co-integration is required in many modern communication systems to reduce size, power, and cost.

NEW GATE STACK PROCESSES AND MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND FRONT END PROCESSES]

Reduction of the equivalent gate oxide thickness has emerged as the most difficult challenge associated with the future device scaling. Higher dielectric constant (high-κ) and metal gate electrode will be required beginning in ~2008. Timely implementation will involve dealing with numerous challenging issues, including appropriate tuning of metal gate work

function, ensuring adequate channel mobility, and gate stack integrity. High-κ scalability in integrated devices below 5 angstroms also remains a critical challenge due to interfacial layer control and availability of higher-κ materials. Impact on mobility and gate dielectric leakage are key issues to be addressed in this highly scaled EOT regime. Furthermore, reliability requirements for high-κ, including dielectric breakdown characteristics (hard and soft breakdown), transistor instability (charge trapping, work function stability, metal ion drift, or diffusion), etc., must be resolved.

Continued DRAM scaling requires construction of memory capacitors in ever-smaller cell area, while maintaining the memory capacitance of 25–35 fF to ensure reliability of stored data. This has resulted in the introduction of dielectric materials with a high dielectric constant (high-κ), such as aluminum oxide, aluminates (for example, HfAlOx) and tantalum oxide, along with a 3D memory structure. Capacitor dielectric thickness scalability for stacked DRAM and trench DRAM need resolution by year 2010 and 2014, respectively. The aspect ratio of stacked DRAM structures also needs resolution by year 2010.

In Flash memory devices, on the other hand, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. This difficult trade-off problem hinders scaling, suggesting the need to introduce high-κ material and 3D structure devices into Flash memory processing. Along with scaling issue of ferroelectric material in FeRAM, new process integration and 3D capacitors will continue to pose major challenges in the development of memory applications.

32 AND 22 NM HALF PITCH [LITHOGRAPHY]

32 nm half pitch is a crucial turning point for lithography imaging scheme. The 193 nm water immersion process is limited with NA to resolve this pitch, unless tight pitches are split into larger ones by double pattering or exposure; however the lithography cost will almost double. Single exposure requires higher-index immersion fluid and lens material. These technologies are still in development. Similarly, high-power sources, fast resists, masks, and related infrastructures are under development for EUV lithography, which also can use single exposures. Multiple-e-beam maskless lithography, which has the potential to bypass mask difficulties and provide manufacturing flexibility, is in an early-stage of development. Timing, cost, defects, critical dimension uniformity (CDU), overlay accuracy, and resists are other increasing issues.

For 22 nm half-pitch lithography, water-immersion 193 nm scanners and double patterning will be severely stretched with extremely large mask error factor, wafer line edge roughness, and design rule restrictions. High-index fluid and lens material will relieve these just a little, if they become available in time. The numerical aperture of EUV systems will have to be raised to more than 0.35 to have the k_1 factor comparable to NA 0.25 for 32 nm half pitch. There is a likelihood of increasing the number of mirrors in the imaging lens, thus leading to requirement of even higher power source while limiting throughput loss, thus less favorable economy. Multiple-e-beam maskless lithography will be better developed by that time but it has to support a high writing rate or more parallelism to maintain the increased pixel count within the same field size. If the potential is realized to keep the per-pass exposure and processing cost as well as the footprint similar to that of mask-based exposure tools, then it will be the most economical and sought-after solution for logic and memory applications.

MASKS [LITHOGRAPHY]

The mask technology is becoming very expensive and challenging. Mask cost has escalated each generation. Increased resolution plus larger mask error enhancement factor (MEEF), due to higher levels of reticle enhancement technology (RET), make the mask CDU and placement accuracy difficult to meet. Mask feature sizes becoming sub-resolution coupled with finite absorber thickness and polarized illumination worsen the problem. Extreme ultraviolet (EUV) masks have further stringent requirements of defect-free ultra-flat substrate and exposure without a pellicle. Inspecting advanced masks is expensive and time consuming. The inspection resolution is reaching limits with practical inspection wavelengths.

RESISTS [LITHOGRAPHY]

Line edge roughness (LER) of photoresist has substantially sustained the same absolute value and therefore has attained an even larger percentage of CD. As pattern geometry shrinks, shot noise starts to become an issue. Resist collapse after development limits its height-to-width aspect ratio to between 2.5 and 3, thus reducing the absolute resist thickness at each technology generation advancement. With immersion lithography, resist material development has to ensure low resist-induced defectivity, further restricting material choices.

CD AND L_{EFF} CONTROL [FRONT END PROCESSES, LITHOGRAPHY AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

With the aggressive scaling of gate length, control of CD has been one of the most difficult issues in lithography and etching. In particular, resist slimming and profile-control of the sidewall, which are commonly utilized to minimize the dimension of effective gate length (L_{eff}), have made CD control far more difficult. Although the acceptable 3-sigma variation of the gate length is shared by lithography and etching at an optimum ratio, the tolerances in both technologies are approaching their limits. In addition, it is becoming very difficult to suppress LER, which depends on gate material, photoresist type, and etch chemistry, even by the optimum control of resist printing and etching. CD control and LER measurement also pose challenges to metrology in terms of accuracy and efficiency. Since off-current between source and drain may be affected by the LER, targets for controlling LER should be set with understanding the impact of LER on device performance. Moreover, the introduction of new gate materials and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy with the controlled sidewall features.

With the aggressive scaling of gate length, control of CD in lithography and etching continues to be a critical bottleneck. In particular, 1) resist slimming 2) gate pitch scaling 3) annealing uniformity, 4) offset spacers, and 5) new gate stack material (metal/high-κ) have made CD and effective gate length control more difficult. Controls of self-aligned doping profile in tight poly pitch and thermal activation uniformity (pattern/layout dependencies) are critical to achieve well-controlled L_{eff}. Gate patterning (lithography and etch) to attain 3-sigma variation of the physical gate below 12% may require the inception of restrictive design rules posing corresponding constraints and challenges to strain engineering and design. Furthermore suppression of LER, critical to minimize device variability, challenges gate materials and integration schemes, as well as etch chemistry processes. Moreover, the introduction of multiple gate and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy, and is limited with the controlled sidewall features.

INTRODUCTION OF NEW MATERIALS TO MEET HIGH CONDUCTIVITY AND LOW DIELECTRIC PERMITTIVITY REQUIREMENTS [INTERCONNECT]

To minimize signal propagation delay and power consumption, the industry has introduced high-conductivity metal and low-permittivity dielectric through damascene processes at 130 nm. The continued scaled-down interconnect poses increasing challenges to technology development and manufacturing. To meet the acceleration of MPU product introduction to a two and a half-year cycle for the next two technology generations (2007 and 2009, and then revision to a three-year cycle after 2009), the fast introduction of new metal/dielectric systems becomes critical. Today, the metal challenges include the fast rising resistivity of narrow Cu wires due to electron scattering at the Cu/barrier metal or dielectric interfaces and the grain boundary. In addition, a very thin and conformal low-resistivity barrier metal is required to integrate with Cu to achieve low resistivity and good reliability. For low-κ dielectrics, good mechanical, chemical, thermal, and physical properties are needed for manufacturable integration with other processes that may induce damage, in particular dry and wet etching, ashing, sputtering, and polishing. Furthermore, low-κ material must have sufficient mechanical strength to survive dicing, packaging, and assembling.

ENGINEERING MANUFACTURABLE INTERCONNECT [INTERCONNECT]

The integration of conductive and low-κ material must meet material, geometrical, planarity, and electrical requirements. Defect, variability, and cost must be engineered to ensure a manufacturable process. The advancement of interconnect should address performance, power, and reliability issues for traditional scaling or equivalent scaling with functional diversity. Since material solutions with traditional scaling cannot deliver performance, new technology has been proposed in recent years including 3D (including tight pitch through silicon vias (TSV)) or air gap structures, different signaling methods, novel design and package options, emerging interconnect using different physics and radical solutions, etc. The realization of these innovative technologies challenges new material systems, process integration, CMOS compatibility, metrology, predictive modeling, and optimization tools for interconnect/packaging architecture design.

POWER MANAGEMENT [DESIGN]

Cost-effective heat removal from packaged chips remains almost flat in the foreseeable future. In addition with the 2× increase in transistor count per generation, power management is now the primary issue across most application segments. Power management challenges need to be addressed across multiple levels, especially system, design, and process technology. Circuit techniques to contain system active and leakage power include multiple V_{dd} domains, clock distribution optimization, frequency stepping, interconnect architectures, multiple V_t devices, well biasing, block shutdowns among others. The implementation challenges of these approaches expand upwards into system design requirements, the continuous improvements in CAD design tools for power optimization (including design robustness against process variability), and downwards into leakage and performance requirements of new device architectures.

Circuit Element and System Modeling for High Frequency (up to 160 GHz) Applications

Accurate and efficient compact modeling of non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling will be of prime importance. Computer-efficient inclusion of statistics (including correlations) before process freeze into circuit modeling is necessary, treating local and global variations consistently. To support concurrent optimization of devices and circuits, efficient building block/circuit-level assessment using process/device/circuit simulation must be supported. Compact models are needed for III-V-, CMOS- and HV- devices. Compact scalable models for passive devices are needed for varactors, inductors, high-density capacitors, transformers, and transmission lines. The parameter extraction for RF compact models preferably tries to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Extreme RF applications like 77 GHz car radar approach the 100 GHz range. Third harmonic distortion for 40 GHz applications implies modeling of harmonics up to 120 GHz. Modeling of effects that have a more global influence gains in importance. Examples are cross talk, substrate return path, substrate coupling, EM radiation, and heating. CAD-tools must be further enhanced to support heterogeneous integration (SoC+SiP) by simulating mutual interactions of building blocks, interconnect, dies and package dealing with possibly different technologies while covering and combining different modeling and simulation levels as well as different simulation domains.

Front-End Process Modeling for Nanometer Structures [Modeling and Simulation]

This is the key challenge for the prediction of result from device fabrication. It overlaps to some extent with the challenge "Ultimate nanoscale CMOS simulation capability", which also includes materials and device simulation. Most important and challenging in the area of front-end process modeling is the modeling of ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants. As an alternative the formation of doped epitaxial layers must be simulated, including their shape and morphology, defect status, and stress. Due to the strongly reduced thermal budgets needed for shallow junctions, that process is highly transient and is governed by the diffusion and reaction of dopant atoms and defects, and especially by the dynamics of clusters of these two. Implantation damage, amorphization, re-crystallisation, and silicidation must be accurately simulated. Anisotropy in models and parameters potentially introduced by thin layers must be investigated. In view of the need to increase carrier mobilities in the channel, the modeling of stress and strain and their influence on diffusion and activation has become vital, especially for strained silicon, SiGe, and for SOI structures. Moreover, stress history and memorization during process sequences is important and must be simulated. Model development, calibration, and evaluation as well as process characterization require numerous experimental activities and large progress in the metrology for dopants, defects, and stress, especially regarding two- and three-dimensional measurements. To enable efficient and accurate three-dimensional simulation, meshing for moving boundaries needs to be strongly enhanced. This challenge is being addressed below in the subchapter on Front-End Process Modeling.

Cost-Effective Manufacturing

Design Productivity and Design for Manufacturing [Design]

The number of available transistors double every technology cycle, increasing design complexity as well. In order to maintain design quality even after process technologies advance, design implementation productivity must be improved to the same degree as design complexity is scaled. Improving design productivity and IP reuse are key considerations for this issue. Challenges at high-level abstraction, platform-based design, multiprocessor programmability, design verification, analog and mixed-signal circuit synthesis are critical to secure design productivity scaling at a pace consistent with process technology cycles. Cost-effective product manufacturing also requires continuous improvements in the area of design for manufacturability, specifically areas such as design for minimization of performance/power sensitivity to device variability and layout styles, lithography-friendly designs, and design for testability and reliability.

Test complexity [Test and Test Equipment]

Several device trends present great challenges to test. Increasing device in/out (IO) bandwidth requirements are rapidly driving the proliferation of faster and wider high-speed interfaces challenging test socket controlled impedance contact limits. Increasing integration of previously disparate semiconductor technologies in SOC or SiP present test challenges in management of per core design for test (DFT), test standardization of SOC core "wrappers" and SiP for example. Emerging technologies such as RF, analog, optical and microelectromechanical systems (MEMs) present some unique test challenges and will require significant improvements in test methods as they become more pervasive or integrated with digital CMOS technologies. Several device architecture trends such as more sophisticated power management or self-repair mechanisms could lead to departure from the longstanding deterministic stored stimulus and response test models and adding higher order dimensionality of test conditions (for example, adding multi-power, multi-voltage, multi-frequency topologies as opposed to single-valued temperature, voltage, and frequency). Test for yield learning is already

critical and is expected to become more so with the introduction of new semiconductor processes and device structures and architectures. Testing for local non-uniformities and detecting symptoms and effects of line width variations, finate dopant distributions, and systematic process defects, are also key challenges to test complexity.

CONTINUED ECONOMIC SCALING OF TEST [TEST AND TEST EQUIPMENT]

The ever-improving economies of scale predicted by Moore's Law may not translate to test naturally. Design for test innovations, widespread use of structural test techniques such as scan testing, and the enabling of higher levels of test parallelism have been very successful in keeping test costs in check to date. However, new test requirements for increasingly complex devices, testing for yield learning, increasing quality requirements, and practical limits on parallel testing continue to present great challenges to test cost. In particular, test tooling cost including probe cards are not scaling and threaten to dominate the total test cost if present trends continue. Accelerating the test learning curve for new device architectures or integration schemes is critical to maintain test cost scaling curve in sync with overall technology cost-scaling goals. Product cost optimization should strike a balance between design, manufacturing, yield learning, and test while securing overall quality of shipped products. Automation of generation entire test programs for automatic test equipment (ATE), convergence of test and system reliability solutions, integration of simulation and modeling of test interfaces hardware and instrumentation into the device design process are challenging opportunities for test cost scaling reduction.

RESPONDING TO RAPIDLY CHANGING COMPLEX BUSINESS REQUIREMENTS [FACTORY INTEGRATION]

Wide ranging business models beyond the integrated device manufacturer (IDM) such as the fabless and foundry model, joint venture, and the variety of task sharing and out-sourcing scenarios have become pervasive in response to customers' rapidly changing complex business requirements. Furthermore, diversified customers' requirement on SoC devices have placed strong demand on manufacturing environments to rapidly and efficiently adapt to high-mix and low-volume product runs. These requirements pose critical near-term challenges in several areas such as integration of larger numbers and different types of equipment, software applications, and fully featured software systems to manage the factory complexity while enabling decreasing time to ramp high volume production.

Development of information exchange/control platform covering all the relevant operation fields, extending from design, mask, front-end-of-line (FEOL), and back-end-of-line (BEOL) to testing, packaging, etc., is also a crucial challenge. Continuous improvements to model factory capacity and performance to optimize output, improve cycle time, and reduce cost are key to successful high-mix factory operations.

IMPROVEMENT IN TRADE-OFF BETWEEN MANUFACTURING COST AND CYCLE TIME [FACTORY INTEGRATION]

Enhanced tool availability, improvements in material handling automation and systems for operational flexibility and control; single-wafer manufacturing; and the reduction/elimination of non product wafers (NPW); are representative areas for continuous improvement in 300 mm lines to meet the challenges of cycle time and cost reduction. The transition from 300 mm to the next wafer size (i.e., 450 mm) is another critical challenge for the semiconductor industry in the 2012–2016 time frame. This transition is considered critical to simultaneously meet the 30% cost/die reduction and a 50% improvement in cycle time.

MEET THE CHANGING COST AND PERFORMANCE REQUIREMENT OF THE MARKET [ASSEMBLY AND PACKAGING]

Many new materials will be introduced in IC packages in the next few years in order to meet requirements of environmental regulations; to improve package performance; and to be compatible with low-κ dielectrics used in Cu interconnects with 45 nm half pitch and beyond. Nano-materials present significant opportunities for the packaging community. The ICs front-end progress is based upon a high level of investment in material and process technology and equipment. There is no corresponding investment in the back-end for materials, process, and equipment. Low-cost opportunities for flip-chip to meet mobile application requirements are challenging and essential, likely requiring new combinations of process and materials. 3D integration (including low-density TVS and via-fill process TVS) and wafer-level packaging, have promises of dramatic cost performance and form factor improvement. The industry will require investment and knowledge of infrastructure to perfect these technologies for high-volume production. The changing marketplace by consumerization of electronic products presents the tremendous opportunity for the packaging industry in implementing 3D integration technologies to fill the gap created by physical limit of Moore's law scaling. Thermal management, thin die handling, signal integrity, and test (as well as environmental issues) are near-term critical challenges for SiP.

SOLUTIONS FOR INTEGRATION OF OFF-CHIP COMPONENTS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS, ASSEMBLY AND PACKAGING]

System-in-package solutions have been developed to meet different applications and system requirements especially in the rapidly changing and increasing market of portable wireless communication devices. The integration of these SiP solutions to construct a universal design platform is increasingly important. High Q RF devices by MEMS or other processes are usually off-chip and need to be made as integrated passive devices (IPD). Three-dimensional stacking and embedded components are two major methodologies to address off-chip components. Forming passive component (as opposed to inserting discrete components) into substrates often involves additional materials such as high-κ dielectric for capacitors, resistive films or paste for resistors, and high permeability (μ) material for inductors. Devising process simplification for this variety of embedded passives is a key challenge to enable a cost-effective alternative. Testing and tuning also pose significant challenges, especially after packaging or assembly processes. Accurate models that include process tolerances as well as circuit and tester parasitic elements are needed for designers to simulate circuit performance with embedded passives before the manufacturing process. Lack of CAD tools for embedded passives also needs to be resolved.

CHEMICAL AND MATERIAL ASSESSMENTS [ESH]

The rapid introduction of new chemicals, materials, and processes requires new rapid assessment methodologies to ensure that new chemicals and materials can be utilized in manufacturing without inducing new hazardous impacts on human health, safety, and the environment. Although methodologies are needed to meet the evaluation and quantification demands for ESH impacts, the focus is currently on expediting process implementation. As such, near-term challenges should include the reduction of emissions from processes using global warming potential (GWP) chemicals.

RESOURCE CONSERVATION [ESH]

As the industry grows and its technology advances toward finer patterning and larger wafer sizes, the natural tendency is toward increased use of water, energy, chemicals, and materials. Resource conservation is becoming a major concern with respect to availability, cost reduction, manufacturing location, sustainability, and waste disposal. Thus, it is necessary to develop diverse process equipment capable of utilizing resources efficiently. Continuous improvement is needed in chemicals and materials utilization and energy consumption reduction in facilities and processing equipment, as well as in efficient thermal management of clean rooms.

DETECTION OF MULTIPLE KILLER DEFECTS AND SIGNAL-TO-NOISE RATIO [YIELD ENHANCEMENT]

Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes required by technology cycles. Inspection sensitivity can be increased to address defect size trends; however challenges arise in terms of efficiently and cost-effectively differentiating defects of interest (DOI) from a vast amount of nuisance and false defects. Reduction of background noise from detection units and samples are key challenges to enhance signal to noise ratio for defect delineation.

LAYOUT STYLE AND SYSTEMATIC YIELD LOSS: HIGH THROUGHPUT LOGIC DIAGNOSIS CAPABILITY [YIELD ENHANCEMENT]

The irregularity of features makes logic areas very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window. Solutions exist but need continuous improvements. Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different automatic test pattern generation (ATPG) flows accommodation; ATE architecture that lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die.

WAFER EDGE AND BEVEL CONTROL AND INSPECTION [YIELD ENHANCEMENT]

Defects and process problems around wafer edge and wafer bevel are known to cause yield problems. Development and continuous improvement in terms of defect detection, throughput, and cost of ownership (CoO) of wafer edge and bevel defect inspection tools are increasingly critical to yield enhancement in advance device technologies.

FACTORY-LEVEL AND COMPANY-WIDE METROLOGY INTEGRATION [METROLOGY]

Metrology areas should be carefully chosen and sampling must be statistically optimized for process control based on cost of ownership (CoO). *In situ* and inline metrology has become requisite for both tight process control and throughput. Information from all metrology (i.e., online and offline), associated with advanced process control (APC), fault detection and classification (FDC), and other systems should be integrated into an efficient database for determining process control

parameters and key correlations to drive yield enhancement. Such efficient and seamless integration requires that standards for process controllers and interfaces, data management and the database structure be established. Continuous improvement of sensors, including calibration, sensing method, and data processing is clearly expected. Development of new sensors must also be concurrently done with the development of advanced process modules.

MEASUREMENT OF COMPLEX MATERIAL STACKS, INTERFACIAL PROPERTIES, AND STRUCTURES [METROLOGY]

Metal-gate high-κ gate stacks, advanced strain and mobility enhancement techniques, as well as advanced interconnect and low-κ dielectric structures require novel or continuous improvement of measurement methodologies and standards in terms of critical dimensions, and physical and electrical properties including interface characteristics. Metrology of film stacks for both front-end and back-end generally provide average physical or electrical property behavior from large area test structures. Therefore, new metrology techniques capable of characterizing stack structures at near nominal dimensions are also needed in the near term. These techniques should be compatible with bulk or SOI substrates. Critical dimension metrology including line edge roughness plays an increasing critical role in process control and variability reduction efforts.

FRONT END PROCESS METROLOGY [METROLOGY]

The device community has shown that CMOS-like transistors, which are referred to as non-classical CMOS, are likely to be the switching device that will be manufactured over the next fifteen years. The process and device design architecture dictate the final selection of metrology requirements. Metrology development is challenged to meet the requirements posed by the accelerated introduction of new technology generations. This requires accelerated advancement of metrology for transistor development and fabrication. Process integration issues such as variability, the need to control leakage current, and the reduction in threshold voltage and gate delay and their tolerances will interact with the reality of process control ranges for gate dielectric thickness doping profiles, junctions, and doses to device metrology needs. Modeling studies of manufacturing tolerances continue to be a critical tool for transistor metrology strategy. CD control and LER measurement also pose challenges to metrology in terms of accuracy and efficiency. Since off-current between source and drain may be affected by the LER, targets for controlling LER should be set with understanding the impact of LER on device performance.

CRITICAL METROLOGY CONSIDERATION—PRECISION AND UNCERTAINTY [METROLOGY]

When comparing measurements with numbers in the roadmap, there are several important considerations. The validity of the comparison is strongly dependent upon how well those comparisons are made. The conventional interpretation of the ITRS precision has been in terms of the single tool reproducibility. The term “precision” is best understood in broader terms as *uncertainty*. Measurement error is a complex function of time (reproducibility), tool (tool-to-tool matching) and sample (sample-to-sample bias variation). The measurement uncertainty is thus defined by the total bias variation with measurement-to-measurement, tool-to-tool and sample-to-sample components. These components may be of varying importance depending on the instrument and the application.

LITHOGRAPHY METROLOGY [METROLOGY]

Lithography metrology continues to be challenged by rapid advancement of patterning technology. A proper control of the variation in transistor gate length starts with mask metrology. Indeed, larger values for mask error factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology has to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimension and overlay are also becoming more challenging. The metrology needs for process control and product disposition continue to drive improvements in precision, relative accuracy, and matching. Acceleration of research and development activities for CD and overlay are essential if to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability which is another important metrology challenge.

IN THE LONG TERM (~2016 THROUGH 2022)

ENHANCING PERFORMANCE

MANAGEMENT OF LEAKAGE POWER CONSUMPTION [DESIGN]

While power consumption is an urgent challenge, its leakage or static component will become a major industry crisis in the long term, threatening the survival of CMOS technology itself, just as bipolar technology was threatened and eventually disposed of decades ago. Leakage power varies exponentially with key process parameters such as gate length, oxide thickness and threshold voltage; this presents severe challenges in light of both technology scaling and variability.

Off-currents in low-power devices increase by a factor of 10 per generation, with emphasis on a combination of drain and gate leakage components. Therefore design technology must be the key contributor to maintain constant or at least manageable static power.

IMPLEMENTATION OF ADVANCED, NON-CLASSICAL CMOS DEVICE WITH ENHANCED DRIVE CURRENT [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

To continue MOSFET scaling to less than L_g = 9 nm, it is quite likely that the device structure will change to advanced non-classical CMOS such as multiple-gate. In these devices, various "technology boosters," such as mobility enhancement by strained Si, elevated source source/drain, high-κ gate dielectric, and metal gate electrode, will likely be simultaneously implemented with the new device structure. Toward the end of the Roadmap timeframe, devices will increasingly be operated in the quasi-ballistic mode, where the current gain will be enhanced by parameters different from those currently known. Eventually, nanowires, carbon nanotubes, and other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed. Choice of the optimum device structures, their physical characterization, and construction of cost-effective processing flows will become very important along with construction of their circuit architecture.

SCALING OF MOSFET [FRONT END PROCESSES]

Continued CMOS scaling trend forecasts the introduction of new materials and new device structures in conjunction with booster technologies such as strain, hybrid-orientation-technique. Non-classical CMOS structure (multi-gate) must be prepared together with advanced FEP processes such as gate stack, junction and silicide. High-κ dielectric EOT must be continuously scaled below 1.0 nm for metal gates while maintaining high reliability with an acceptable leakage current. Both low sheet resistance and process productivity must be retained, while junction depth will be aggressively scaled. Parasitic resistance must be controlled by introducing a new silicide metal or a new structure such as a Schottky junction. Gate CD variation must be suppressed by process optimization of lithography, photoresist trim, and gate etch.

SHIFTING FROM TRADITIONAL SCALING TOWARD EQUIVALENT SCALING AND FUNCTIONAL DIVERSITY THROUGH UNCONVENTIONAL APPROACHES [INTERCONNECT]

Even with the projected improvements in materials and processes, traditional scaling alone is deemed to be insufficient to meet interconnect performance requirements in the long term. The challenge will be to achieve equivalent scaling by adopting nontraditional technologies as well as new design and architectures. Among the technologies nearing production, 3D integration by the use of TSVs would enable construction of highly complex systems without making global interconnects unduly long. Wireless signaling with passive devices might broaden design and integration options. Looking further into the future, innovative materials and/or wiring schemes, such as carbon nanotubes and/or optical wiring, could significantly raise the performance limits set by metal/dielectric interconnects. Also along the lines of departure from simple scaling, the possibility of adding functional diversity using novel interconnects needs to be explored. Possible technologies in this direction include, for example, embedded repeaters, variable-resistor vias, and integrated back-end memory. In implementing these new technologies, use of unconventional materials such as compound semiconductors should not be precluded. However, it is most desirable to realize functional integration by developing CMOS-compatible interconnect processes and the necessary metrology.

GATE CD CONTROL IMPROVEMENTS AND PROCESS CONTROL [LITHOGRAPHY]

With aggressive scaling of devices, the required gate CD control comes down to 0.92 nm in 3σ with a line width reduction (LWR) of less than 1.2 nm in 3σ in 2016 for every lithography potential solution. (Please note that Si-Si lattice distance is 0.235 nm.) Furthermore, resolution and precision measurements for CD down to 4.5 nm, including LWR metrology of 0.36 nm in 3σ is very challenging, along with the required overlay accuracy of 2.2 nm in 3σ or better in 2022. The maximum permissible defect size on patterned wafer is reduced to smaller than 6.6 nm in 2022. Without metrology and inspection tools having sufficient accuracy and resolution, CD control improvements and process control will be difficult to achieve.

NON-DESTRUCTIVE PRODUCTION MEASUREMENTS [METROLOGY]

Non-destructive (without charging or contaminating the surface) and high-resolution wafer/mask level microscopy for measuring the critical dimensions of 3D structures is required. The relationship between the physical object and the waveform analyzed by the instrument should be understood to improve CD measurement including physical feature measurement. Surface charging and contamination need to be improved as well as sensor and sensing method. New design of optics with aberration correction is required for high resolution and better throughput. Ion microscopy is also one of the candidate technologies to cope with this subject. The combination of high-resolution optics, waveform

analysis, and non-charging technique enables precise grasp of 3D structures for CD measurement. At the same time, CD metrology tool must be calibrated by using standard reference material or structure for reliable and stable measurement.

Continuous CMOS Scaling, Heterogeneous Integration, and Beyond CMOS [Emerging Research Devices]

There are three technological approaches for continuous functional scaling of information processing technologies to the 16 nm generation and beyond. The continuous CMOS scaling is attained by developing new materials to replace silicon as an alternate channel to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation. The heterogeneous integration is aiming at developing practice new device technologies and primitive-level architectures to provide special purpose optimized functional cores heterogeneously integrated with silicon CMOS. The "beyond CMOS" approach will invent and develop a new information processing technology eventually to replace CMOS.

Control of Nanostructures and Properties [Emerging Research Materials]

One of Emerging Research Materials's (ERM's) most difficult challenges is to deliver material options with controlled and desired properties. These material options must exhibit the potential to enable high density emerging research devices, lithographic technologies, and interconnect fabrication and operation at the nanometer scale. This challenge requires not only the control of nanostructure properties such as size, bandgap etc., but also placement of nanostructures, such as carbon nanotubes (CNTs), nanowires, or quantum dots, in precise locations for devices and interconnects. To improve the control of material properties for nanometer (nm) scale applications, collaboration and coordination within the research community are required.

Cost-Effective Manufacturing

Test for Yield Learning [Test]

Test's peripheral role as a feedback loop for understanding underlying defect mechanisms, process marginalities, and as an enabler for rapid fabrication process yield learning and improvement has traditionally been considered a secondary role to screening hard defects. With the increasing reduction in feature (and defect) sizes well below optical wavelengths, rapidly increasing failure analysis throughput times, reduction in failure analysis efficacy, and approaching practical physical limits to other physical techniques (pica, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of DFT and test-enabled diagnostics and yield learning becomes paramount.

Emerging New Packaging [Assembly and Packaging]

In 2016 integrated circuits will see M1-half pitch of 23 nm in MPU/ASIC, core voltage of 0.5 V, and I/O frequency of 35 GHz for high performance applications. These device characteristics will rely on advanced packaging technology and new packaging materials for incorporation into electronic systems. Potential solutions for high heat generation and hot spot phenomena include advanced fluidic cooling systems and new generation of high thermal conductive materials such as carbon nanotubes based material. Broad band data transfer may require guided wave optical interconnects or some other high speed electrical interface built into the package. Organic or biological devices emerging in the market will require biological interfaces. From the system design view point, the integration of a wide variety of devices in SiP will require improved design tools and methodology to achieve optimal partitioning.

Meeting Process Requirements at 32 nm and Beyond Generations Running Production Volumes [Factory Integration]

Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory continues to be a primary challenge. Small process windows and tight process targets at 32 nm generations in many modules force decision makings in process control increasingly complex and difficult that will have a large impact to the factory information and control system. Especially quality tracking and control in even higher mix with smaller lot size operations will become one of the primary production efficiency limiters.

Modeling of Chemical, Thermomechanical, and Electrical Properties of New Materials [Modeling and Simulation]

Increasingly new materials need to be introduced in technology development due to physical limits that otherwise would prevent further scaling. This introduction is required especially for gate stacks, interconnect structures, and photoresists, and furthermore for Emerging Research Devices. In consequence, equipment, process, device, and circuit models must be extended to include these new materials. Furthermore, computational material science needs to be developed and applied to contribute to the assessment and selection of new materials in order to reduce the experimental effort, and to contribute to the databases required for semi-empirical calculations.

DEVELOPMENT OF MODEL-BASED DESIGN-MANUFACTURING INTERFACE [YIELD ENHANCEMENT]

In the future it will be necessary to develop model-based design-manufacturing interfaces. Due to optical proximity correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc. It will be necessary to develop test structures that address complex integration issues of new technology generations. Statistical methodology should also be incorporated with the interface to cope with ever increasing transistor counts.

CHEMICAL AND FACILITY MANAGEMENT BY ESH DESIGN AND MEASUREMENT METHODS [ESH]

Equipment design engineers and equipment users require timely information regarding ESH characteristics of potential new process chemicals and materials and method. This information is essential to the proper selection of optimal chemicals and materials and methods for minimization of ESH impact. Chemical data availability and chemical assessment is essential to the proper evaluation for new process. And the conservation of facilities energy and water and material is essential to the minimization of global environmental impact. To minimize the ESH impact without delaying process implementation, integrated ESH design and measurement and evaluation methods needs to be developed.

WHAT IS NEW FOR 2007— THE WORKING GROUP SUMMARIES

SYSTEM DRIVERS

WHAT'S NEW?

The 2007 System Drivers Chapter continues to evolve to include market-driven drivers that reflect the demands of a 21st-century roadmap. These driver segments include the following:

- *Networking*: NEW for 2007, this driver represents the class of chips that are used in high bandwidth communications applications. Power efficiency and multi-core design are increasingly used in this application.
- *Consumer stationary driver*: Introduced in the 2006 update, this driver represents a high-performance version of the increasingly important consumer electronics market.
- *Consumer mobile driver*: Existing since the 2005 version, this driver represents a huge class of chips that rely on extremely power efficient techniques for battery-powered devices.
- *Office / MPU*: An "old" existing driver, it has been updated in its modeling of clock frequency growth and growth in the number of cores on chip to reflect current realities in power-limited microprocessor design.
- *Other* existing drivers have been reviewed to ensure the direction is appropriate.
- *Additional* drivers are being examined for inclusion in future roadmaps, including medical and automotive drivers.

A complete set of market-driven drivers is thus being formed for the System Drivers roadmap, to fully align the ITRS with other chapters; the electronic industry, and with other system-level roadmaps such as iNEMI.

An analysis of "More than Moore" aspects has also been pursued, focusing on the consumer portable driver and compared with "*emulators"* in the iNEMI system level roadmap. The long-term goal is to match system-level and chip-level requirements on a driver basis. This analysis is shown in the chapter as well.

Table ITWG1 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
I. Portable/consumer			
1. Size/weight ratio: peak in 2004 2. Battery life: peak in 2004 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount Need SOC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
II. Medical			
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 months 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
III. Networking and communications			
1. Bandwidth: 4×/3–4 years 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m^3 of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions

IV. Defense			
1. Cost: not prime concern 2. Time-to-market: >12 months 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
V. Office			
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m^3 4. Form factor: shrinking size 5. Reliability	Large gate counts; high speed Drives demand for digital functionality Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog; simple A/D and D/A Video i/f for automated camera monitoring, video conferencing Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-position resolution	MPU cores and some specialized functions Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
VI. Automotive			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software	Cost-driven on-chip A/D and D/A for sensor and actuators Signal processing shifting to DSP for voice, visual Physical measurement ("communicating sensors" for proximity, motion, positioning); MEMS for sensors	

A/D—analog to digital ASSP—application-specific standard product D/A—digital to analog DEMUX—demultiplexer DSP—digital signal processing FPGA—field programmable gate array i/f—interface I/O—input/output HW—hardware MEMS—microelectromechanical systems MUX—multiplexer RTOS—real-time operating system

DESIGN

WHAT'S NEW?

After going through a major revision in the 2005 edition, the 2006 design chapter update featured a full quantitative design technology roadmap. The 2007 Design chapter focuses on providing meaningful updates of some of the figures, dates, and challenges, including moderate revisions of the System-Level, Verification, DFM, and Logic/Circuit/Physical Design sections.

Most sections now include a table that relates challenges and solutions. Although a one-on-one relationship is usually not warranted, it is quite helpful in certain parts of the design flow. The 2008 version of this chapter will continue in this direction while increasingly accounting for alternative integration methods that add on to Moore's Law (heterogeneous systems, system-in-package (SIP), etc.).

Indeed, an "inventory" analysis of "More than Moore" design technology aspects has also been pursued, looking at the design technology solutions aligned with each design technology section (system level, logic/circuit/physical, verification, DFT, DFM). This analysis is shown in the chapter as well.

DIFFICULT CHALLENGES

While the 2007 Design chapter still lists five overall design technology challenges, design productivity, closely linked to system and design process complexity, and of course affecting design cost, is the most massive and critical challenge, both in the short and long term, and is affected by the other four challenges. The second through fifth challenges are narrower in scope, and mostly address silicon complexity issues. From those challenges, the most critical are power consumption and manufacturability:

- Power consumption is an urgent, short-term challenge, quickly shifting from a performance-driven active power crisis to a variability-driven leakage power crisis in the long term. Power consumption is classified as an "enhancing performance" type challenge in the ITRS Executive summary.
- Manufacturability, i.e., the ability to produce a chip in large quantities at acceptable cost and according to an economically feasible schedule, has been affecting the industry primarily due to lithography hardware limitations but will become a major crisis in the long term as variability in its multiple forms invades all aspects of a design. Manufacturability is classified as a "cost-effective manufacturing" type challenge in the ITRS Executive Summary.

Table ITWG2 Overall Design Technology Challenges

Challenges ≥ 32 nm	*Summary of Issues*
Design productivity	System level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification Logic/circuit/layout: analog circuit synthesis, multi-objective optimization
Power consumption	Logic/circuit/layout: dynamic and static (leakage), system and circuit, power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/layout: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/layout: signal integrity analysis, EMI analysis, thermal analysis
Challenges <32 nm	*Summary of Issues*
Design productivity	Complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage Tools specific for SOI and non-static logic, and emerging devices Cost-driven design flow Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	SOI power management
Manufacturability	Uncontrollable threshold voltage variability Advanced analog/mixed signal DFT (digital, structural, radio), “statistical” and yield-improvement DFT Thermal BIST, system-level BIST
Reliability	Autonomic computing, robust design, SW reliability
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)

ATE—automatic test equipment BISR—built-in self repair BIST—built-in self test DFT—design for test
EMI—electromagnetic interference ESL—Electronic System-level Design HW/SW—hardware/software
MTTF—mean time to failure SOI—silicon on insulator

TEST AND TEST EQUIPMENT

WHAT'S NEW?

The 2007 Test chapter was originally planned as a refinement of the 2005 Test chapter, but has evolved into including major changes. The 2005 chapter contained some overlapping information in various sections and every effort has been made in the 2007 chapter to eliminate overlap in sections. As an example, the SoC table was completely redefined to only refer to issues pertaining to testing integrations of cores. Core specific requirements are covered in the Logic, Memory, Mixed signal, etc, tables. This resulted in an increase of readability and usability of the SoC table and further drove the need for each of the core tables to be self contained. Consumer logic has been added to the 2007 Logic table whereas the 2005 Logic table focused on only high volume microprocessors and omitted consumer requirements.

In other changes for 2007, DRAM, Flash, and Embedded memory tables have now been combined into a single memory table and embedded SRAM, which was identified as a gap in the 2005 roadmap, and has been added for 2007. The DRAM portion of the memory table is based on a new model and shows significant increases in the I/O data rate over the 2005 information. I/O data rates on commodity DRAM devices will increase to over 8 Gb/s by 2022.

There are significant additions in 2007. RF and test socket tables have been added. The three handler tables of the 2005 roadmap for logic, communication devices, and memory have been combined into a single table, but divided into three areas based upon DUT power consumption. The prober table now represents the needs for all device types versus the logic only focus of the 2005 tables. A new section has been added for specialty devices such as LCD display drivers, imaging devices and other high-volume devices that are required for consumer and mobile applications but are not covered in the other sections. Specialty devices can drive requirement that are beyond the requirements specified in the other tables.

Finally, many table colors have been changed for 2007 based upon a new method of determining colors and table value entries. The value in the each of the table cells was determined by the requirements of the silicon manufacturers based upon the expected needs of the devices. The colors of the cell are the equipment supplier response to the stated need.

KEY TEST DRIVERS, DIFFICULT CHALLENGES, AND OPPORTUNITIES

Table ITWG3 Summary of Key Test Drivers, Challenges, and Opportunities

Key Drivers (not in any particular order)	
Device trends	Increasing device interface bandwidth (# of signals and data rates) Increasing device integration (SoC, SiP, MCP, 3D packaging) Integration of emerging and non-digital CMOS technologies Complex package electrical and mechanical characteristics Device characteristics beyond one sided stimulus/response model Multiple I/O types and power supplies on same device Multiple digital I/O types on same device
Increasing test process complexity	Device customization during the test process "Distributed test" to maintain cost scaling Feedback data for tuning manufacturing Dynamic test flows via "Adaptive Test" Higher order dimensionality of test conditions
Continued economic scaling of test	Physical limits of test parallelism Managing (logic) test data and feedback data volume Defining an effective limit for performance difference for HVM ATE versus DUT Managing interface hardware and (test) socket costs Trade-off between the cost of test and the cost of quality Multiple insertions due to system test and BIST
Difficult Challenges (in order of priority)	
Test for yield learning	Critically essential for fab process and device learning below optical device dimensions
Detecting Systemic Defects	Testing for local non-uniformities, not just hard defects Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects

Screening for reliability	Implementation challenges and efficacies of burn-in, IDDQ, and Vstress Erratic, non deterministic, and intermittent device behavior
Potential yield losses	Tester inaccuracies (timing, voltage, current, temperature control, etc) Over testing (e.g., delay faults on non-functional paths) Mechanical damage during the testing process Defects in test-only circuitry or spec failures in a test mode e.g., BIST, power, noise Some IDDQ-only failures Faulty repairs of normally repairable circuits Decisions made on overly aggressive statistical post-processing
Future Opportunities (not in any order)	
Test program automation (not ATPG)	Automation of generation of entire test programs for ATE
Simulation and modeling	Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process
Convergence of test and system reliability solutions	Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMs—micro-electromechanical systems

PROCESS INTEGRATION, DEVICES AND STRUCTURES

WHAT'S NEW?

The *Process Integration, Devices, and Structures (PIDS)* chapter addresses overall IC process flow integration, with the main IC devices and structures, and with the reliability trade-offs associated with new options. Physical and electrical requirements and characteristics are emphasized within PIDS, encompassing parameters such as physical dimensions, key device electrical parameters, including device electrical performance and leakage, and reliability criteria. The focus is on nominal targets, although statistical tolerances are discussed as well. Key technical challenges facing the industry in this area are addressed, and some of the best-known potential solutions to these challenges are discussed. The chapter is subdivided into the following major subsections: logic, memory (including both DRAM and non-volatile memory [NVM]), and reliability.

Key aims of the ITRS include both identifying key technical requirements and challenges critical to sustaining the historical scaling of CMOS technology per Moore's Law and stimulating the needed research and development to meet the key challenges. The objective of listing and discussing potential solutions in this chapter is to provide the best current guidance about approaches that address the key technical challenges. However, the potential solutions list is not comprehensive, nor are the solutions in the list necessarily the most optimal ones. Given these limitations, the potential solutions in the ITRS are meant to stimulate and not limit research exploring new and different approaches.

LOGIC

A major portion of semiconductor device production is devoted to digital logic. In this section, both high-performance and low-power logic (typically for mobile applications) are included, and detailed technology requirements and potential solutions are considered for both types. Key considerations are performance, power, and density requirements and goals. One key theme is continued scaling of the MOSFETs for leading-edge logic technology in order to maintain historical trends of improved device performance. This scaling is driving the industry toward a number of major technological innovations, including material and process changes such as high-κ gate dielectric, metal gate electrodes, etc., and in the long term, new structures such as ultra-thin body, multiple-gate MOSFETs (such as FinFETs). These innovations are expected to be introduced at a rapid pace, and hence understanding, modeling, and implementing them into manufacturing in a timely manner is expected to be a major issue for the industry

MEMORY

Logic and memory together form the predominant majority of semiconductor device production. The types of memory considered in this chapter are DRAM and non-volatile memory (NVM). The emphasis is on commodity, stand-alone chips, since those chips tend to drive the memory technology. However, embedded memory chips are expected to follow the same trends as the commodity memory chips, usually with some time lag. For both DRAM and NVM, detailed technology requirements and potential solutions are considered

The NVM discussion in this chapter is limited to devices that can be written and read many times; hence read-only memory (ROM) and one-time-programmable (OTP) memory are excluded. The current mainstream types of NVM currently is Flash, both NAND and NOR. There are serious issues with scaling that are dealt with at some length in the chapter. Other, non-charge-storage types of NVM are also considered, include ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase change RAM. For DRAM type memory, the key issue is dealing with increasing scaling difficulties, especially with ensuring very low levels of leakage.

RELIABILITY

Reliability is a critical aspect of process integration. Emerging technology generations require the introduction of new materials and processes at a rate that exceeds current capabilities for gathering information and generating the required database and models on new failure regimes and defects. Because process integration must then be performed without the benefit of extended learning, it will be difficult to maintain current reliability levels. Uncertainties in reliability can also lead to unnecessary performance, cost, and time-to-market penalties. These issues place difficult challenges on testing and wafer level reliability (WLR). Packaging interface reliability is particularly vulnerable to reliability problems because of new materials and processes, form factors, tighter lead and bond spacing, severe environments, adhesion, and customer manufacturing capability issues.

DIFFICULT CHALLENGES

Table ITWG3 Process Integration Difficult Challenges—Near-term Years

Difficult Challenges ≥ 22 nm	*Summary of Issues*
1. Scaling of MOSFETs to the 22 nm technology generation	Scaling planar bulk CMOS will face significant challenges due to the high channel doping required, band-to-band tunneling across the junction and gate-induced drain leakage (GIDL), random doping variations, and difficulty in adequately controlling short channel effects. Also, keeping parasitics, such as series source/drain resistance with very shallow extensions and fringing capacitance, within tolerable limits will be significant issues. Implementation into manufacturing of new structures such as ultra-thin body fully depleted silicon-on-insulator (SOI) and multiple-gate (e.g., FinFET) MOSFETs is expected at some point. This implementation will be challenging, with numerous new and difficult issues. A particularly challenging issue is the control of the thickness and its variability for these ultra-thin MOSFETs, as well as control of parasitic series source/drain resistance for very thin regions.
2. With scaling, difficulties in inducing adequate strain for enhanced mobility.	With scaling, it is critically important to maintain (or even increase) the current significantly enhanced CMOS channel mobility attained by applying strain to the channel. However, the strain due to current process-induced strain techniques tends to decrease with scaling.
3. Timely assurance for the reliability of multiple and rapid material, process, and structural changes	Multiple major changes are projected over the next seven years, such as.: Material: high-κ gate dielectric, metal gate electrodes, lead-free solder Process: elevated S/D (selective epi) and advanced annealing and doping techniques Structure: ultra-thin body (UTB) fully depleted (FD) SOI, multiple-gate MOSFETs, multi-chip package modules It will be an important challenge to ensure the reliability of all these new materials, processes, and structures in a timely manner.
4. Scaling of DRAM and SRAM to the 22 nm technology generation	DRAM main issues with scaling—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs. SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities and soft error rate with scaling. Also, difficult lithography and etch issues with scaling.
5. Scaling high-density non-volatile memory to the 22 nm technology generation	Flash—Non-scalability of tunnel dielectric and interpoly dielectric. Dielectric material properties and dimensional control are key issues. FeRAM—Continued scaling of stack capacitor is quite challenging. Eventually, continued scaling in 1T1C configuration. Sensitivity to IC processing temperatures and conditions. MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions

Table ITWG3 Process Integration Difficult Challenges—Long-term Years

Difficult Challenges<22 nm	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate MOSFETs) with ultra-thin, lightly doped body will be needed to scale MOSFETs to 10 nm gate length and below effectively. Control of parasitic resistance and capacitance will be critical. To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, nanowires, carbon nanotubes, or other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed.
7. Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs	Fundamental issues of statistical fluctuations for sub-10 nm gate length MOSFETs are not completely understood, including the impact of quantum effects, line edge roughness, and width variation.
8. Identifying, selecting, and implementing new memory structures	Dense, fast, low operating voltage non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness and attaining the very low leakage currents and power dissipation that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc.) are currently unclear. For detail, refer to ITRS Interconnect chapter.
10. Eventually, identification, selection, and implementation of advanced, non-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of non-CMOS devices need to extend well beyond CMOS limits. Non-CMOS devices need to integrate physically or functionally into a CMOS platform. Such integration may be difficult. See Emerging Research Devices sections for more discussion and detail.

[1] Scaling of MOSFETs to the 22 nm technology generation—With scaling of planar bulk MOSFETs, the channel doping will need to be increased to undesirably high levels in order to gain adequate control of short-channel effects and to set the threshold voltage properly. As a result of the high channel doping, the mobility of holes and electrons will be reduced and the junction leakage due to band-to-band tunneling and gate-induced drain leakage will increase. Furthermore, due to the small total number of dopants in the channel of extremely small MOSFETs, the percent stochastic (random) variation in the number and location of the dopants will increase sharply, and this will sharply increase the statistical variability of the threshold voltage. Another challenge for highly scaled MOSFETs is reducing the parasitic series source/drain resistance (R_{sd}) to tolerable values with very shallow source and drain junction depth.

Due to the challenges with scaling planar bulk MOSFETs, advanced devices such as ultra-thin body fully depleted SOI MOSFETs and multiple-gate, particularly double-gate (DG) MOSFETs (e.g., FinFETs) are expected to be eventually implemented. Since such devices will typically have lightly doped channels and the threshold voltage will be controlled by the metal gate electrode's work function, the challenges associated with high channel doping and stochastic dopant variation in planar bulk MOSFETs will be avoided, but numerous new challenges are expected. Amongst the most critical of such challenges will be controlling the body thickness and its variability for these ultra-thin structures, and setting the metal gate electrode work function to its desired value. As with the planar bulk MOSFET, it will be highly challenging to reduce the parasitic series source/drain resistance (R_{sd}) to tolerable values, but here the ultra-thin body is an added difficulty.

With scaling, a common issue for both planar bulk and advanced MOSFETs is expected to be increased line edge roughness as a percentage of the gate length.

For high-performance logic, in the face of increased chip complexity and increasing transistor leakage current with scaling, chip static power dissipation is expected to become particularly difficult to control while at the same time meeting aggressive targets for performance scaling. Innovations in circuit design and architecture for performance management, as well as utilization of multiple transistors on chip, are needed to design chips with both the desired performance and power dissipation. The multiple transistors have different threshold voltages (V_t), with the low V_t, high

leakage devices used mainly in the critical paths, and higher V_t, lower leakage devices used in the rest of the chip. For low-power logic, control of static power dissipation with scaling is the critical goal. To meet this goal, the transistor leakage current is projected to be much lower than for high-performance logic, and circuit and architectural innovations as well as multiple transistors on the chip will be needed, similarly to high-performance logic.

[2] With scaling, difficulties in inducing adequate strain for enhanced mobility—Currently enhanced channel mobility due to applied strain to the channel is a major contributor to meeting the MOSFET performance requirements. With scaling, it is critically important to maintain (or even increase) the significantly enhanced CMOS channel mobility to continue to meet the performance requirements. However, the strain due to current process-induced strain techniques tends to decrease with scaling, and solutions to maintain the strain in scaled structures are needed. (For more detail, see Logic Potential Solutions section.)

[3] Timely assurance for the reliability of multiple and rapid material, process, and structural changes—In order to successfully scale ICs to meet performance, leakage current, and other requirements, it is expected that numerous major process and material innovations, such as high-κ gate dielectric, metal gate electrodes, elevated source/drain, advanced annealing and doping techniques, new low-k materials, lead-free solders, multi-chip packages, etc., will need to be implemented in well under a decade. Also, it is projected that new MOSFET structures, starting with ultra-thin body SOI MOSFETs and moving on to ultra-thin body, multiple-gate MOSFETs, will need to be implemented. Understanding and modeling the reliability issues for all these innovations so that their reliability can be ensured in a timely manner is expected to be particularly difficult.

[4] Scaling of DRAM and SRAM to the 22 nm technology generation—For DRAM, a key issue is implementation of high-κ dielectric materials and eventually MIM structures in order to get adequate storage capacitance per cell even as the cell size is shrinking. Also important is controlling the total leakage current, including the dielectric leakage, the storage junction leakage, and the access transistor source/drain subthreshold leakage, in order to preserve adequate retention time. The requirement of low leakage currents causes problems in obtaining the desired access transistor performance. Finally, deploying of low sheet resistance materials for word and bit lines to ensure acceptable speed for scaled DRAMs is critically important.

For SRAM, difficulties with scaling are expected, particularly in maintaining both acceptable noise margins and controlling instability, especially hot electron instability and negative bias temperature instability (NBTI). Also, there are difficult lithography and etch issues with scaling, and difficult issues with keeping the leakage current within tolerable targets for highly scaled SRAMs. Solving these SRAM challenges is critical to system performance, since SRAM is typically used for fast, on-chip memory.

[5] Scaling high-density non-volatile memory (NVM) to the 22 nm technology generation—Inherent in the nature of available nonvolatile semiconductor memory are two challenges. The first is that the memory element structure for each NVM technology differs from the underlying CMOS technology in some way, and accommodating those differences while attempting to scale the memory cell poses some difficult issues. These issues vary depending on which NVM technology is being considered, and specific issues are listed for each NVM type in the table. The second challenge is that the normal operating process used to set and to reset the state of the memory cell generally stresses the materials, and degradation of cell characteristics can be expected. Degradation is usually associated with a defect related mechanism rather than with an intrinsic device characteristic. Endurance and retention requirements provide the user with guidance as to the probable capability of the device and define a "safe" range of use. For both parameters it is a continuous challenge to be able to realistically predict this long-term behavior. Failure causes are difficult to identify and real-time testing is not feasible.

[6] Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs—For the long-term years, when the transistor gate length is projected to become 10 nm and below, ultra-thin body, multiple-gate MOSFETs with lightly doped channels are expected to be utilized to effectively scale the device, and particularly, to control short-channel effects for such highly scaled devices. The other material and process solutions mentioned above, such as high-κ gate dielectric, metal gate electrodes, strained silicon channels, elevated source/drain, etc., are expected to be incorporated along with the non-classical CMOS structures. For 10 nm gate length and below, body thicknesses well below 10 nm are projected, and the impact of quantum and surface scattering effects on such thin devices are not well understood. Finally, for these advanced, highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal carrier velocity and injection at the source end appears to be necessary. Eventually, high transport channel materials, such as germanium or III-V channels on silicon, or carbon nanotubes or nanowires, may be utilized.

[7] Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs—For such devices, the impact of statistical variations is not well understood, including the impact of quantum effects, line edge roughness, and variation in the ultra-thin body width.

[8] Identifying, selecting, and implementing new memory structures—In the long term, increasing difficulty is expected in scaling both DRAMs and NVMs, as discussed for each of these memory types in the table. The need for high density, fast, and new non-volatile memory structures is expected to increase, particularly to reduce power dissipation. Implementing such advanced, non-volatile structures will be a major challenge.

[9] Identifying, selecting, and implementing novel interconnect schemes—The resistivity of copper increases somewhat with scaling for widths under ~100 nm, and at κ ~1–1.5, the limits of low-κ dielectric will be reached. At that point, further interconnect performance improvements will require novel architectural and/or materials solutions

[10] Eventually, identification, selection, and implementation of advanced, non-CMOS devices and architectures for advanced information processing—Eventually, toward the end of the Roadmap or beyond, scaling of MOSFETs is likely to become ineffective and/or very costly, and advanced non-CMOS solutions will need to be implemented to continue to improve performance, power, density, etc. It is expected that such solutions will be integrated either functionally or physically with a CMOS baseline technology that takes advantage of the high-performance, cost-effective, and very dense CMOS logic that will have been developed and implemented by then.

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

WHAT'S NEW?

RF AND AMS CMOS

- RF CMOS requirements for millimeter-wave that are linked to the high-performance CMOS roadmap with a two-year lag.
- RF parameters for F_t, F_{max}, and noise figures at 24 GHz and 60 GHz

RF AND AMS BIPOLAR DEVICES

- Considered three separate bipolar devices—high voltage for typical low-cost bipolar devices, high speed for millimeter-wave applications, and power amplifiers.
- The focus is on high speed and power amplifiers as drivers.
- High speed device F_t scaling is less aggressive. Delayed 300 GHz by one year and 500 GHz by five years and adjusted F_{max}, J_C and BV_{CEO} scaling accordingly.
- Revised power amplifier NPN parameters and aligned them to power amplifier battery voltages
- Added noise figures at 60 GHz

ON CHIP AND EMBEDDED PASSIVES FOR RF AND ANALOG

- Added the three applications of analog, RF, and power amplifier
- Included such devices as capacitors, resistors, inductors, and varactors
- Added the metal-oxide-metal capacitor

POWER AMPLIFIERS (0.8 GHZ–10 GHZ)

- Handset—For HBT and FET based handsets that use III-V compounds and Si, added end-of-life battery voltage, FET-HBT integration for integrated bias circuit designs, and on-chip switch integration for by-passing intermediate frequency stages. The emerging markets are demanding that power amplifiers be either cost/performance driven or cost-only driven applications. Cost-only markets are driving silicon single chip alternatives.
- Base Station**—**Included cellular and the emerging worldwide interoperability for microwave access (WiMAX) that require relatively high RF power and LDMOS and III-V FET devices.
- Removed SiC devices because they are being displaced by GaN devices.

MILLIMETER WAVE (10 GHZ–100 GHZ)

- Now dominated by III-V devices (GaAs PHEMT, InP HEMT, GaAs MHEMT, GaN HEMT, InP HBT) and SiGe HBT and RF CMOS.
- Emphasized low noise amplifiers and power devices

MORE THAN MOORE FOCUS OF WIRELESS - MULTI-STANDARD APPLICATIONS

- Addressed multi-band, multi-mode, portable applications
- Because the device roadmap alone does not enable the software defined radio (SDR), added the needs to address digital radio design requirements by using a hybrid approach with wideband amplifiers and matching, filtering, and switching networks
- Added two new tables on embedded passives requirements and RFMEMS requirements.

DIFFICULT CHALLENGES

Table ITWG4 RF and Analog Mixed-Signal (RF and AMS) Technologies for Wireless Communications Difficult Challenges

Difficult Challenges	*Summary of Issues*
Radio Integration	Performance and cost trade-offs for SoC versus SiP solutions Signal isolation and integrity are challenges to technologists, designers, and EDA tool providers for both analog and digital domains CAD solutions for integrated radio SiP designs (chip, passive, MEMS, package, tool compatibility, and model accuracies)
Device Technology	Optimizing analog/RF CMOS devices with scaled technologies. Fundamental changes in CMOS device structure may lead to the need for separate process/chip to support conventional precision analog/RF devices Increasing Ft of silicon bipolar devices by more aggressive vertical profiles Managing higher current and power densities that result from aggressive vertical profiles in silicon bipolar devices Performance and cost trade-offs for integrating passive devices Predictability of battery technology (end-of-life) and its impact on PA roadmap Compound semiconductor substrate quality, reliability, thermal management, particularly for GaN Low-cost processing equipment for compound semiconductors
Design	Design approach for wider range of supply voltages Digitizing analog functions in the software define radio (SDR) Non-linear and 3D Electromagnetic models for accurate design and simulation Computationally efficient physical models for compound semiconductors Thermal modeling and simulations that are integrated with RF and digital design tools.

EMERGING RESEARCH DEVICES

WHAT'S NEW?

The new 2007 Emerging Research Devices (ERD) chapter has been changed and broadened compared to the 2005 ERD chapter. The section on Emerging Research Materials, prominent in 2005, has been expanded to include new materials for lithography, assembly and packaging, FEP, and interconnect in addition to Emerging Research Devices to form a separate new chapter on Emerging Research Materials (ERM). Materials research issues related to emerging devices are summarized in this ERD chapter and treated more fully in the new ERM chapter. The other major change is increased focus on emerging research device technologies that can be integrated with a CMOS platform technology to extend CMOS further into existing markets and to open new applications.

This possibility motivates an expansion in scope and content of the Emerging Research Devices chapter for 2007. The chapter evaluates emerging new research technologies for memory and information processing or logic devices and nano-architectures applied to two different approaches to realizing integrated electronic functions. One is heterogeneous integration of these new technologies with the CMOS platform, i.e., "enhanced CMOS" or "Functional Diversification". The second addresses the exciting but daunting challenge to invent one or more fundamentally new approaches to information and signal processing. This theme will require discovery and exploitation of a new means to physically represent, process, store, and transport information via new materials, process, device, nano-architecture, and systems innovations.

In the Memory section, Nanofloating Gate Memory has been removed from ERD and recommended to PIDS, and the Resistance-based Memory has been replaced with the Fuse/Antifuse Memory, the Ionic Memory, the Electronic Effects Memory, and the Macromolecular Memory (formerly the Polymer Memory). A new entry for Nanomechanical Memory has also been added.

In addition to broadening the scope of the Logic section to include alternative information processing device structures for supplementing/complementing CMOS, this section also expands the technology entry for 1D structures into a new category entitled "FET Extension". This category includes a new technology entry on "Channel Replacement" materials. These materials are proposed to replace silicon in the channel to enhance carrier mobility and velocity to enable scaling CMOS to the end of the Roadmap. Examples of channel replacement materials are Ge, SiGe, and III-V compound semiconductor materials. Development of graphene ribbon material for MOSFET application has also been added to the 1D or low dimensional category for enhanced FETs.

Finally, the Architecture section has been broadened and re-structured to include emerging research architectures utilizing, for special purposes, novel devices other than CMOS to perform unique functions. Here we use the term *architecture* to refer to a functional arrangement on a single chip of interconnected devices that includes embedded computational components. Implicit in this formulation is the assumption that these devices can be integrated with CMOS structures that will continue to perform many of the generic computational and Input/Output functions required of the implementation. This section explores device and architectural trends to give visibility to architectural options and attempt to establish criteria for weighing alternative approaches.

DIFFICULT CHALLENGES

Table ITWG5 Emerging Research Device Technologies Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile and non-volatile memory technologies to and beyond 22 nm	SRAM and FLASH scaling will reach definite limits within the next several years (see PIDS chapter for Difficult Challenges). These are driving the need for new memory technologies to replace SRAM and FLASH memories. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM
Difficult Challenges <22 nm	
Scale CMOS to and beyond the 16 nm technology generation.	Develop new materials to replace silicon as an alternate channel to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation for technology scaled to 16 nm and beyond. Candidate materials include Ge, SiGe, III-V compound semiconductors, and graphene. Develop 1D (nanowire or nanotube) structures to scale MOSFETs and CMOS gates beyond the 16 nm technology generation. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.)
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and a primitive-level architecture to provide special purpose optimized functional cores heterogeneously integrable with silicon CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and develop a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. Bridge a knowledge gap that exists between materials behaviors and device functions.

EMERGING RESEARCH MATERIALS

WHAT'S NEW

The 2007 Emerging Research Materials (ERM) chapter is a new addition to the ITRS (previously a section in the 2005 and 2006 ERD chapter). The scope of ERM 2005–2006 was materials to support ERD, but the ERM chapter now also assesses ERM for lithography, front end process, interconnects, and assembly and package applications. The ERM chapter also identifies metrology, modeling, and environmental safety and health research needed to support these materials for their potential applications. While these ERMs have properties that make them attractive as potential solutions to future technology needs, significant progress is required for them to be used in future technologies.

Low dimensional materials, such as nanotubes, nanowires, and other nanoparticles, and macromolecules, have properties that could provide solutions for emerging research devices, lithography, front end process, interconnects, and assembly and packaging. Self-assembled materials have potential for applications in lithography, to enable high charge density capacitors, and for selective deposition or etching processes in front end processes. Spin materials are of primary interest for emerging research device applications. Complex metal oxides have potential for applications as emerging research memory and logic devices. A special set of the complex metal oxides, strongly correlated electron state materials, and their heterointerfaces may have potential to enable new logic devices with coupled spin and charge properties. The challenges for these materials the required metrology, modeling, and environmental safety and health research needed are highlighted in the difficult challenges table.

DIFFICULT CHALLENGES

The current set of sub-22 nm ERM Difficult Research Challenges is summarized in Table 1. Perhaps ERM's most difficult challenge is to deliver material options, with controlled and desired properties, in time to impact insertion decisions. These material options must exhibit the potential to enable high density emerging research devices, lithographic technologies, and interconnect fabrication and operation at the nanometer scale. This challenge, to improve the control of material properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community. Accelerated synthesis, metrology, and modeling initiatives are needed to enhance targeted material-by-design capabilities and enable viable emerging material technologies. Improved metrology and modeling tools also are needed to guide the evolution of robust synthetic methods for these emerging nanomaterials. The success of many ERMs depend on robust synthetic methods that yield useful nanostructures, with the required control of composition, morphology, an integrated set of application specific properties, and compatibility with manufacturable technologies.

To achieve high density devices and interconnects, ERMs must assemble in precise locations, with controlled orientations. Another critical ERM factor for improving emerging device, interconnect, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties. For novel nanometer scale materials emerging within the research environment, methodologies and data also must be developed that enable the hierarchical assessment of potential environment, safety, and health impact of new nanomaterials and nanostructures.

Table ITWG6 Emerging Research Material Technologies Difficult Challenges

Difficult Challenges ≤ 22 nm	*Summary of Issues*
Control of nanostructures and properties	Ability to pattern sub 20nm structures in resist or other manufacturing related patterning materials (resist, imprint, self assembled materials, etc.) Control of surfaces and interfaces Control of CNT properties, bandgap distribution and metallic fraction Control of stoichiometry and vacancy composition in complex metal oxides Control and identification of nanoscale phase segregation in spin materials Control of growth and heterointerface strain Ability to predict nanocomposite properties based on a "rule of mixtures" Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability Control of interface properties (e.g., electromigration)
Control of self assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components Control of line width of self-assembled patterning materials Control of registration and defects in self-assembled materials
Characterization of nanostructure-property correlations	Correlation of the interface structure, electronic and spin properties at interfaces with low-dimensional materials Characterization of low atomic weight structures and defects (e.g., carbon nanotubes, graphitic structures, etc.) Characterization of spin concentration in materials Characterization of vacancy concentration and its effect on the properties of complex oxides 3D molecular and nanomaterial structure property correlation
Characterization of properties of embedded interfaces and matrices	Characterization of the electrical contacts of embedded molecule(s) Characterization of the roles of vacancies and hydrogen at the interface of complex oxides and the relation to properties Characterization of transport of spin polarized electrons across interfaces Characterization of the structure and electrical interface states in complex oxides
Compatibility with CMOS processing	Integration for device extensibility Material compatibility and process temperature compatibility
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures Device structure-related properties, such as ferromagnetic spin and defects Dopant location and device variability

The difficult challenges listed in Table 6 may gate the progress of the emerging research materials considered in this chapter. Significant methodology development is needed that enables material optimization and projected performance analysis in different device structures and potential application environments. Hence, the importance of significant collaboration between the synthesis, characterization, and modeling communities cannot be over stated. Material advances require an understanding of the interdependent relationships between synthetic conditions, the resulting composition and structure, and their impact on the material's functional performance. Thus, characterization methods must be sufficient to establish a quantitative relationship between composition, structure, and functional properties. Furthermore, it must enable model validation and help to accelerate the optimization of the required materials properties. This implies the need for strong alignment between experimentalists and theorists, when establishing a knowledge base to accelerate the development of ERM related models and potential applications.

FRONT END PROCESSES

WHAT'S NEW?

Continued performance improvement through equivalent scaling has manifested itself in Front End Processes as "material-limited device scaling." Traditional transistor and capacitor formation materials, silicon, silicon dioxide, and polysilicon have been pushed to fundamental material limits and continued scaling has required the introduction of new materials. In addition, new approaches to device structure, such as non-planar multi-gate devices, will be needed for future performance scaling

Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures. In addition, the end of planar bulk CMOS is becoming visible within the next several years. As a consequence we must be prepared for the emergence of CMOS technology that uses non-conventional MOSFETs or alternatives such as planar fully depleted SOI (FDSOI) devices and dual- or multi-gate devices either in a planar of vertical geometry. Projections for the manufacturing introduction of non-conventional MOSFET devices are 2010 for FDSOI and 2011 for multi-gate. The challenges associated with integration of these diverse new materials and structures are the central theme of the FEP difficult challenges.

Combined with the extension of silicon oxynitride gate dielectric materials and the introduction of strain-enhanced-mobility channels, the need for high-κ had been delayed, but is now upon us. It is expected that leading manufacturers will start production of high-κ gate dielectrics in 2008. Mobility enhancement and channel-length scaling, which requires accelerated scaling of junctions to control short channel effects, will continue to provide enhanced device performance. It is also expected that dual metal gates, having appropriate work functions, will be put in production by leading manufacturers in 2008 to replace the dual doped polysilicon gates, currently the mainstay of CMOS technology.

The introduction of new materials is also expected to impose added challenges to the methods used to dope and activate silicon. In addition to the scaling imposed need for producing very shallow highly activated junctions, the limited thermal stability of most high-κ materials is expected to place new boundaries on thermal budgets associated with dopant activation. In a worst-case scenario, the introduction of these materials could have a significant impact on the overall CMOS process architecture.

In the memory area, high-κ materials are now in use for both stacked and trench DRAM capacitors. DRAM stacked capacitors are also now using metal-insulator-metal (MIM) structures with trench capacitors projected to move to MIM by 2010. It is expected that high-κ materials will be required for the Floating Gate Flash memory interpoly dielectric by 2010 and for tunnel dielectric by 2013. FeRAM will make a significant commercial appearance where ferroelectric and ferromagnetic storage materials would be used. The introduction of these diverse materials into the manufacturing mainstream is viewed as important, difficult challenges. In addition, phase-change memory (PCM) devices are expected to make a commercial appearance by 2010.

In the starting wafer area, it is expected that alternatives to bulk silicon such as silicon-on-insulator substrates will proliferate. Additionally, various forms of strained silicon technology may be incorporated although these have been and continue to be principally achieved through value-added modifications to the IC manufacturing process. Also, an important difficult challenge expected to emerge within the Roadmap horizon is the potential need for the next generation 450 mm silicon substrate. Based upon historical diameter change cycles, the industry is already several years behind the pace necessary to allow the next generation 450mm silicon substrate to be ready for device manufacture in the year 2012.

Front end cleaning processes will continue to be impacted by the introduction of new front end materials such as high-κ dielectrics, metal gate electrodes and mobility-enhanced channel materials. Scaled devices are expected to become increasingly shallow, requiring that cleaning processes become completely benign in terms of substrate material removal and surface roughening. Scaled and new device structures will also become increasingly fragile, limiting the physical aggressiveness of the cleaning processes that may be employed. Also, there is a challenge for particle scanning technology to reliably detect particles smaller than 28nm on a wafer surface for characterization of killer defect density and to enable yield learning.

DIFFICULT CHALLENGES

Table ITWG7 Front End Processes Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Starting Materials	1.5 mm edge exclusion FDSOI Si and buried oxide thickness control SOI defectivity levels Full production of 450 mm wafer size
Surface Preparation	Critical surface particle size below 28 nm not measurable on wafer Ability to achieve clean surfaces while controlling material loss and surface damage
Thermal/Thin Films/Doping/Etch	Introduction of high-κ/metal gate into high performance (HP) and low operating/low standby power (LOP/LSTP) and equivalent oxide thickness (EOT) scaling below 0.8 nm Increasing device performance with strain engineering and applying it to FDSOI and multi-gate technologies Scaling extension junction depths below 10 nm while achieving high dopant activation Achieving manufacturable interfacial contact resistivities below 10^{-7} Ω-cm^2 to meet parasitic series resistance requirements Si thickness and control for FDSOI and Multi-gate Gate critical dimension control for physical gate length < 20 nm Introduction of new channel materials with high interface quality and low processing thermal budget
DRAM	Improvement of oxide etching capability for high aspect ratio (>40) storage node formation in stack capacitor and for oxide hardmask for high aspect ration trench capacitor. Improvement of Si etching capability for high A/R (>90) trench capacitor formation. Continued scaling of stacked and trench capacitor dielectric Teq below 0.5 nm Continued scaling of physcial dielectric thickness (tphys) while maintaining high dielectric constant (>90) and low leakage current of dielectric
Non-volatile Memory	Scaling of IPD Teq to <6Å for NAND and NOR Scaling of tunnel oxide thickness to <8Å for NOR Scaling of STI fill aspect ratio to >9 starting for NAND PCM material conformality of ≥90% PCM minimum operating temperature of 125°C PCM resistivity change and reset current density Integration and scaling of FeRAM ferroelectric materials Continued scaling of FeRAM cell structure
Difficult Challenges < 22 nm	*Summary of Issues*
Starting Materials	1.5 mm edge exclusion FDSOI Si and buried oxide thickness control SOI defectivity Surface particles
Surface Preparation	Surface particles not measurable Ability to achieve clean surfaces while controlling material loss and surface damage Metrology of surfaces that may be horizontally or vertically oriented relative to the chip surface Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface Achievement and maintenance of structural, chemical, and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface
Thermal/Thin Films/Doping/Etch	Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation. Continued EOT scaling below 0.7 nm with appropriate metal gates Gate CD Control
DRAM	Continued scaling of capacitor structures for both stacked and trench type as well as continued scaling of dielectric thickness
Non-volatile Memory	Floating gate Flash technology considered unscalable beyond 22 nm—new Flash NVM technology will be required Continued scaling of phase change memory technology Continued scaling of FeRAM technology

LITHOGRAPHY

DIFFICULT CHALLENGES

Table ITWG8 Lithography Difficult Challenges

*Difficult Challenges ≥ 32 nm**	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Registration, CD, and defect control for masks
	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features
	Understanding polarization effects at the mask and effects of mask topography on imaging and optimizing mask structures to compensate for these effects
	Eliminating formation of progressive defects and haze during exposure
	Determining optimal mask magnification ratio for <32 nm half pitch patterning with 193 nm radiation and developing methods, such as stitching, to compensate for the potential use of smaller exposure fields
	Development of defect free 1× templates
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time
	Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume
	Sufficient lifetime for exposure tool technologies
	Resources for developing multiple technologies at the same time
	ROI for small volume products
	Stages, overlay systems and resist coating equipment development for wafers with 450 mm diameter
Process control	Processes to control gate CDs to < 1.3 nm 3σ
	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3σ overlay error
	Controlling LER, CD changes induced by metrology, and defects < 10 nm in size
	Greater accuracy of resist simulation models
	Accuracy of OPC and OPC verification, especially in presence of polarization effects
	Control of and correction for flare in exposure tool, especially for EUV lithography
	Lithography friendly design and design for manufacturing (DFM)
Immersion lithography	Control of defects caused in immersion environment, including bubbles and staining
	Resist chemistry compatibility with fluid or topcoat and development of topcoats
	Resists with index of refraction > 1.8
	Fluid with refractive index > 1.65 meeting viscosity, absorption, and fluid recycling requirements
	Lens materials with refractive index >1.65 meeting absorption and birefringence requirements for lens designs
EUV lithography	Low defect mask blanks, including defect inspection with < 30 nm sensitivity and blank repair
	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components
	Resist with < 3 nm 3σ LWR, < 10 mJ/cm2 sensitivity and < 40 nm ½ pitch resolution
	Fabrication of optics with < 0.10 nm rms figure error and < 10% intrinsic flare
	Controlling optics contamination to achieve > five-year lifetime
	Protection of masks from defects without pellicles
Double patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures
	Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
	Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
	Photoresists with independent exposure of multiple passes
	Fab logistics and process control to enable low cycle time impact that include on-time availability of additional reticles and efficient scheduling of multiple exposure passes

**Lithography challenges ≥32nm versus the convention of the 2007 ITRS for challenges of ≥22nm will be reviewed in the 2008 Update.*

Table ITWG8 Lithography Difficult Challenges (continued)

*Difficult Challenges < 32 nm**	*Summary of Issues*
Mask fabrication	Defect-free masks, especially for 1× masks for imprint and EUVL mask blanks free of printable defects
	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair), especially for 1× masks
	Mask process control methods and yield enhancement
	Protection of EUV masks and imprint templates from defects without pellicles
	Phase shifting masks for EUV
Metrology and defect inspection	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3σ
	Metrology for achieving < 2.8 nm 3σ overlay error
	Defect inspection on patterned wafers for defects < 30 nm, especially for maskless lithography
	Die-to-database inspection of wafer patterns written with maskless lithography
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective optical and post-optical masks
	Achieving ROI for industry with sufficient lifetimes for exposure tool technologies and ROI for small volume products
Gate CD control improvements and process control	Development of processes to control gate CD < 0.9 nm 3σ with < 1.2 nm 3σ line width roughness
	Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3σ overlay error, especially for imprint lithography
	Process control and design for low k1 optical lithography
Resist materials	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Limits of chemically amplified resist sensitivity for < 32 nm half pitch due to acid diffusion length
	Materials with improved dimensional and LWR control

**Lithography challenges <32nm versus the convention of the 2007 ITRS for challenges of <22nm will be reviewed in the 2008 Update.*

INTERCONNECT

WHAT'S NEW?

Over the past four decades the primary drivers for conventional metal dielectric interconnects have been technology scaling and the desire for increased performance. During this timeframe, interconnect wiring has evolved from a single level of Al/SiO_2 wiring to eleven levels of Cu/low-κ interconnect in the current generations. In the near term, the most difficult challenge for interconnect is the introduction of new materials that meet the wire conductivity requirements and reduce the dielectric permittivity. Future effective κ requirements preclude the use of a trench etch stop for dual damascene structures. This is an additional impediment to achieving tight control of pattern, etch and planarization of metal wires to reduce RC variability. At < 22 nm, feature size effects, such as electron scattering from grain boundaries and interfaces, will continue to increase the effective Cu resistivity. Ultra low-κ dielectrics may be replaced by air gaps in selective areas. The accelerated scaling of MPU pitch has aggravated the copper electromigration problem. J_{max} limits for current dielectric cap technologies for copper will be exceeded by 2010. Modification of the Cu surface to form CuSiN, use of alloys such as Cu-Al or implementation of a selective metal cap technology, such as CoWP, will be necessary.

However, even with material changes to improve performance, the difficulties for interconnect technology resulting from scaling can be noted by observing that older 1.0 μm Al/SiO_2 technology had a transistor delay of ~20 ps and the RC delay of a 1 mm line was ~ 1.0 ps, while in a projected 35 nm Cu/low-κ technology, the transistor delay will be ~1.0 ps, and the RC delay of a 1 mm line will be ~250 ps. In addition, at 130 nm half-pitch , approximately 51% of microprocessor power was consumed by interconnect, with a projection that without changes in design philosophy, in the next five years up to 80% of microprocessor power will be consumed by interconnect. In recognition of the increasing importance of the dynamic power dissipated in the interconnect structure, a new power metric was added to the MPU and ASIC Technology Requirements Tables in 2006. The power metric is the power (measured in Watts) dissipated per Ghz of frequency and cm^2 of metal layer. Although the power metric is seen to plateau for the long-term years due to aggressive introduction of low-κ dielectrics, the power dissipated in the interconnect structure will still increase dramatically due to higher frequencies and increases in the number of metal layers.

This dramatic increase of the interconnect impact on performance and power shows clearly the challenges created by the scaling of the conventional metal/dielectric system. In the last few years IC manufacturers have recognized the difficulty of addressing interconnect performance and power issues by technology means alone. In response, they have implemented design and architecture improvements to address interconnect limitations; however, even with these advances, interconnect remains a critical bottleneck for many applications. This creates an ever increasing opportunity for developing and introducing alternative interconnect solutions. In addition to resolving some of the power and performance problems associated with conventional metal/dielectric systems, alternative interconnect technologies offer the potential of increased product functional diversity. For example, optical interconnects might be used with multiple wavelengths in a single waveguide (wavelength-division multiplexing (WDM)) to provide not only higher bandwidth density for global interconnects, but also in combination with on-chip, voltage variable gratings to provide selective routing possibilities that can be used for radically different signal processing functions than those currently available. In recognition of these significant opportunities, the 2007 Interconnect ITRS roadmap includes expanded sections on the status and challenges of three dimensional chip and wafer stacking (3DIC), optical interconnect and carbon nanotubes (CNT).

DIFFICULT CHALLENGES

Table ITWG9 Interconnect Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures, processes and new materials*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges < 22 nm	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address 3D structures and other packaging issues*	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

** Top three challenges*

CMP—chemical mechanical planarization *DRAM—dynamic random access memory*

FACTORY INTEGRATION

DIFFICULT CHALLENGES

Difficult challenges associated with factory integration span multiple technology generations and cut across the five factory thrust areas. Responses to these challenges are often linked to the technology introductions as a matter of industry convenience to minimize disruptions to operating factories. Near-term difficult challenges for the factory include business, technical, and economic issues that must be addressed.

Table ITWG10 Factory Integration Difficult Challenges

Difficult Challenges ≥22 nm	*Summary Of Issues*
Responding to rapidly changing, complex business requirements	Many new and co-existing business models including IDM, foundry, fabless, joint ventures, collaborations, other outsourcing, etc., need to be considered in the Factory Integration Increased expectations by customers for faster delivery of new and volume products Need for improve integration of the entire product design and manufacturing process Faster design → prototype and pilot → volume production Enhanced customer visibility into outsourced production operations Reduced time to ramp factories, products, and processes to stay competitive within the rapidly changing business environment Building 30+ mask layer System on a Chip (SoC) with high-mix manufacturing as the model in response to diversified customers' requirement Rapid and frequent factory plan changes driven by changing business needs Ability to model factory performance to optimize output and improve cycle time for high mix factories Ability to constantly adjust equipment loading to keep the factory profitable Manufacturing knowledge and control information need to be shared as required among disparate factories
Achieving growth targets while margins are declining	Implications of rising wafer, packaging, and other materials cost on meeting cost targets Meeting high factory yield much faster at startup Addressing increased complexity while keeping costs in check Reducing complexity and waste across the supply chain Inefficiencies introduced by non-product wafers (NPW) competing for resources with production wafers High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs Increasing dedication of masks and equipment causing manufacturing inefficiencies Challenges introduced with sharing of mask sets Difficulty in maintaining the historical 0.7× transistor shrink per year for die size and cost efficiency
Managing ever increasing factory complexity	Quickly and effectively integrating rapid changes in process technologies Managing carriers with multiple lots, wafers with multiple products, or multiple package form factors Comprehending increased purity requirements for process and materials Need to run aluminum and copper back end in the same factory Increasing number of processing steps coupled with process and product complexity Need to concurrently manage new and legacy software and systems with increasingly high interdependencies Explosive growth of data collection/analysis requirements driven by process and modeling needs Increased requirements for high mix factories. Examples are complex process control as frequent recipe creation and changes at process tools and frequent quality control due to small lot sizes
Meeting factory and equipment reliability, capability or productivity requirements per the Roadmap	Process equipment not meeting availability, run rate, and utilization targets out of the box Stand alone and integrated reliability for equipment and systems to keep factories operating Increased impacts that single points of failure have on a highly integrated and complex factory Quality issues with production equipment embedded controllers to improve equipment process performance instability and NPW requirements Lack of good data to measure equipment and factory effectiveness for optimization and improvement programs Factory capacity planning and supply chain management systems are not continuously base lined with actual factory data creating errors Small process windows and tight process targets at >45 nm (DRAM contacted half pitch)in many modules make process control increasingly difficult Lack of migration paths which inhibit movement from old inefficient systems to new highly productive systems

Table ITWG10 Factory Integration Difficult Challenges (continued)

Difficult Challenges <22 nm	*Summary of Issues*
Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	Need to quickly convert factories to new process technologies while reusing equipment, facilities, and skills Minimizing downtime to on-going operations while converting factories to new technologies Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] Continued need to improve both throughput and cycle time Reuse of building, production and support equipment, and factory information and control systems across multiple technology generations Understanding up-front costs to incorporate EFS (Extendibility, Flexibility and Scalability) Comprehending increased purity requirements for process and materials Accelerating the pace of standardization to meet industry needs
Meeting process requirements at 65 nm and 45 nm generations running production volumes	Small process windows and tight process targets at 32 nm generations in many modules make process control increasingly difficult Complexity of integrating next generation lithography equipment into the factory Overall development and volume production timelines continuing to shrink Device and process complexity make the ability to trace functional problems to specific process areas difficult Difficulty in running different process parameters for each wafer while maintaining control windows and cycle time goals Reducing the impacts of parametric variation
Increasing global restrictions on environmental issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
Post-conventional CMOS manufacturing uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements will have on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency Need to run CMOS and post CMOS processes in the same factory
Emerging factory paradigm and next wafer size change	Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness. Traditional strategies to scale wafers and carriers for the 450 mm wafer size conversion may not work with [450 mm] 25 wafer carriers and drive significant production equipment and material handling changes Uncertainty concerning how to reuse buildings, equipment, and systems to enable 450 mm wafer size conversion at an affordable cost

ASSEMBLY AND PACKAGING

DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near term difficult challenges exist in all phases of the assembly and packaging process from design through manufacturing, test and reliability.

Many critical technology requirements are yet to be met and they are listed in Table ITWG11 below. Meeting these requirements will demand significant investment in research and development.

Table ITWG11 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥22 nm	*Summary of Issues*
Impact of BEOL including Cu/low κ on packaging	-Direct wire bond and bump to Cu or improved barrier systems bondable pads - Dicing for ultra low k dielectric -Bump and underfill technology to assure low-κ dielectric integrity including lead free solder bump system -Improved fracture toughness of dielectrics -Interfacial adhesion -Reliability of first level interconnect with low κ -Mechanisms to measure the critical properties need to be developed. -Probing over copper/low κ
Wafer level CSP	-I/O pitch for small die with high pin count -Solder joint reliability and cleaning processes for low stand-off -Wafer thinning and handling technologies -Compact ESD structures -TCE mismatch compensation for large die
Coordinated design tools and simulators to address chip, package, and substrate co-design	-Mix signal co-design and simulation environment -Rapid turn around modeling and simulation -Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis -Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) -System level co-design is needed now. -EDA for “native” area array is required to meet the Roadmap projections. -Models for reliability prediction
Embedded components	-Low cost embedded passives: R, L, C -Embedded active devices -Quality levels required not attainable on chip -Wafer level embedded components
Thinned die packaging	- Wafer/die handling for thin die - Different carrier materials (organics, silicon, ceramics, glass, laminate core) impact -Establish infrastructure for new value chain -Establish new process flows -Reliability -Testability -Different active devices -Electrical and optical interface integration

Table ITWG11 Assembly and Packaging Difficult Challenges (continued)

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Close gap between chip and substrate Improved organic substrates	-Increased wireability at low cost -Improved impedance control and lower dielectric loss to support higher frequency applications -Improved planarity and low warpage at higher process temperatures -Low-moisture absorption -Increased via density in substrate core -Alternative plating finish to improve reliability -Solutions for operation temp up to C5-interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology -Production techniques will require silicon-like production and process technologies after 2005 -Tg compatible with Pb free solder processing (including rework at260°C)
High current density packages	-Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. -Whisker growth -Thermal dissipation
Flexible system packaging	-Conformal low cost organic substrates -Small and thin die assembly -Handling in low cost operation
3D packaging	-Thermal management -Design and simulation tools -Wafer to wafer bonding -Through wafer via structure and via fill process -Singulation of TSV wafers/die - Test access for individual wafer/die -Bumpless interconnect architecture
Difficult Challenges <22 nm	*Summary of Issues*
Package cost does not follow the die cost reduction curve	-Margin in packaging is inadequate to support investment required to reduce cost -Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	These devices may exceed the capabilities of current assembly and packaging technology requiring new solder/UBM with: -Improved current density capabilities -Higher operating temperature
High frequency die	-Substrate wiring density to support >20 lines/mm -Lower loss dielectrics—skin effect above 10 GHz -"Hot spot" thermal management There is currently a "brick wall" at five-micron lines and spaces.
System-level design capability to integrated chips, passives, and substrates	-Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. -Complex standards for information types and management of information quality along with a structure for moving this information will be required. -Embedded passives may be integrated into the "bumps" as well as the substrates.
Emerging device types (organic, nanostructures, biological) that require new packaging technologies	-Organic device packaging requirements not yet defined (will chips grow their own packages) -Biological interfaces will require new interface types

TSV—through silicon via

ENVIRONMENT, SAFETY, AND HEALTH

WHAT'S NEW?

- ESH Tables have been completely rewritten
- 2007/8 requirements are primarily focused on setting ESH metric baseline and replace the sliding scale of relative improvements
- Chemical/Materials table and process table are now reflective of ESH goals for initial chemical selection and process parameters respectively (the Process Table is new from 2005).
- Additions for 2007 include ERM requirements and a New Equipment Design section
- All metrics have been evaluated and updated where appropriate
- Potential Solutions Tables have incorporated the elements which are solution oriented but previously contained in the technical requirements tables

DIFFICULT CHALLENGES

Table ITWG12 Environment, Safety, and Health Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Chemicals and materials management	*Chemical Assessment* Evaluation and refinement of quality, rapid assessment methodologies to ensure that new materials such as nanomaterials can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation Regional differences in regulations for chemicals; given regional movement for R&D, pre-manufacturing, and full commercialization Trend towards lowering exposure limits and more monitoring
	Chemical Data Availability Inability to forecast/anticipate future restrictions or bans on materials, especially nanomaterials Lack of comprehensive ESH data for new, proprietary chemicals and materials to respond to the increasing external and regional requirements on the use of chemicals
	Chemical Exposure Management Lack of information on how the chemicals and materials are used and what process by-products are formed Method to obtain information on how the chemicals and materials are used and what process by-products are formed
Process and equipment management	*Process Chemical Optimization* Need to develop equipment and processes that meet technology demands while reducing impact on human health, safety and the environment, both through the use of more benign materials, and by reducing chemical quantity requirements through more efficient and cost-effective process management
	Environment Management Capability for component isolation in waste streams Need to understand ESH characteristics of process emissions and by-products to identify the appropriate mitigation Need to develop effective management systems to address issues related to hazardous and non-hazardous residues from the manufacturing processes
	Global Warming Emissions Reduction Need to reduce emissions from processes using high GWP chemicals
	Water and Energy Conservation Need for innovative energy- and water-efficient processes and equipment

Table ITWG12 Environment, Safety, and Health Difficult Challenges (continued)

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Process and equipment management	*Consumables Optimization* Need for more efficient utilization of chemicals and materials, and increased reuse and recycling
	Byproducts Management Development of improved metrology for byproduct speciation.
	Chemical Exposure Management Need to design-out potential for chemical exposures and the necessity for personal protective equipment (PPE) Design for Maintenance Need to design equipment so that commonly serviced components and consumable items are easily and safely accessed Need to design equipment so that maintenance and service may be safely performed by a single person Need to minimize health and safety risks during maintenance activities.
	Equipment End-of-Life Need to develop effective management systems to address issues related to re-use and disposal of equipment
	Conservation Need to reduce use of energy, water and other utilities Need for more efficient thermal management of clean rooms and facilities systems
Facilities technology requirements	*Global Warming Emissions Reduction* Need to design energy efficient manufacturing facilities Need to reduce total CO_2 equivalent emissions
	Sustainability Metrics Need to identify the elements for defining and measuring the sustainability of a technology generation
Sustainability and product stewardship	*Design for ESH* Need to make ESH a design parameter at the design stage of new equipment, processes and products
	End-of-Life Disposal/Reclaim Need to design facilities, equipment and products to facilitate re-use/disposal at end of life
Difficult Challenges < 22 nm	*Summary of Issues*
Chemicals and materials management	*Chemical Assessment* Evaluation and refinement of quality, rapid assessment methodologies to ensure that new materials such as nanomaterials can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation
	Chemical Data Availability Lack of comprehensive ESH data for new, proprietary chemicals and materials to respond to the increasing external and regional requirements on the use of chemicals
	Chemical Exposure Management Lack of information on how the chemicals and materials are used and what process by-products are formed
	Chemical Reduction Need to develop processes that meet technology demands while reducing impact on human health, safety, and the environment, both through the use of more benign materials, and by reducing chemical quantity requirements through more efficient and cost-effective process management Need to reduce emissions from processes using high GWP chemicals
Process and equipment management	*Environment Management* Need to understand ESH characteristics of process emissions and by-products to identify the appropriate mitigation Need to develop effective management systems to address issues related to hazardous and non-hazardous residues from the manufacturing processes
	Water and Energy Conservation Need to reduce water and energy consumption Need for innovative energy and water-efficient processes and equipment

Table ITWG12 Environment, Safety, and Health Difficult Challenges (continued)

Difficult Challenges < 22 nm	*Summary of Issues*
Process and equipment management	*Consumables Optimization* Need for more efficient utilization of chemicals and materials, and increased reuse and recycling
	Chemical Exposure Management Need to design-out potential for chemical exposures and need for personal protective equipment (PPE)
	Design for Maintenance Need to design equipment so that maintenance and service may be safely performed by a single person Need to design equipment so that commonly serviced components and consumable items are easily accessed Need to minimize health and safety risks during maintenance activities
	Equipment End-of-Life Need to develop effective management systems to address issues related to re-use and disposal of equipment
	Conservation Need to reduce use of energy, water and other utilities Need for more efficient thermal management of clean rooms and facilities systems
Facilities technology requirements	*Global Warming Emissions Reductio*n Need to design energy efficient facilities support equipment and manufacturing facilities. Need to reduce emissions from processes using high GWP chemicals
	Sustainability Metric Need to identify the elements for defining and measuring the sustainability of a technology generation Need to identify the elements for defining and measuring sustainability at a factory infrastructure level Design for ESH Need method to holistically evaluate and quantify the ESH impacts of processes, chemicals, and process equipment for the total manufacturing process Need to make ESH a design parameter in development of new equipment, processes and products End-of-Life Disposal/Reclaim Need to design facilities, equipment, and products to facilitate re-use/disposal at end of life
Sustainability and product stewardship	

YIELD ENHANCEMENT

DIFFICULT CHALLENGES

The difficult challenges for the Yield Enhancement chapter are summarized in Table ITWG13. The detection of multiple killer defect types and simultaneous differentiation at high capture rates, low cost of ownership, and throughput were identified by the community as the most important challenge for yield enhancement. Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes defined by technology generations. The need of higher sensitivity of in-line inspections is leading to a dramatic increase of defect counts. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects. At the same time, a low Cost of Ownership (CoO) of the tools demands for high throughput of the inspection. This is in conflict with the issue of improving the signal-to-noise ratio. The key of successful inspection results are both a high sensitivity and a high capture rate for Defects of Interest (DOI).

The wafer edge and bevel control have a top priority on the list of key challenges. Defects and process problems around wafer edge and wafer bevel were identified to impact yield. It is a key challenge to find the appropriate inspection of wafer edge, bevel, and apex on the wafer front and backside. Defect inspection concepts or technologies are either under development or have to be realized within the next few years.

Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and to determine the required control limits. The issues for this challenge are to define the relative importance of different contaminants to wafer yield, a standard test for yield/parametric effect, and a maximum process variation (control limits). The fundamental challenge is to understand the correlation between impurity concentration in key process steps and device yield, reliability, and performance. This correlation will determine whether further increases in contamination limits are truly required. The challenge increases in complexity as the range of process materials widens and selection of the most sensitive processes for study will be required for meaningful progress.

It is a challenge to effectively identify Systematic Mechanisms Limited Yield (SMLY). The tackling through logic diagnosis capability designed into products and systematically incorporated in the test flow is crucial. The irregularity of features makes logic areas very sensitive to SMLY such as patterning marginalities across the lithographic process window. Before reaching random-defect limited yields, the SMLY should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different Automatic Test Pattern Generation (ATPG) flows to accommodate, Automatic Test Equipment (ATE) architecture that can lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die, and statistical aggregation of diagnosis results for building a layout-dependent systematic yield model.

The use of Scanning Electron Microscope (SEM) Energy Dispersive X-ray (EDX) for in-line chemical analysis has inherent limitations that are magnified, as defects of interest become smaller than 100 nm. Sampling volume is the primary limitation, followed by insufficient bonding information and possible e-beam damage. So tools/techniques are needed for elemental analysis in-line. The focus of required developments is on light elements and small amount of samples, as the need to analyze smaller particle increases with shrinking geometries. This challenge is a crosscut of yield enhancement and metrology issues.

Table ITWG13 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Detection of multiple killer defect types / signal to noise ratio – The detection of multiple killer defect types and simultaneous differentiation at high capture rates, low cost of ownership and throughput is required. The need of higher sensitivity of in-line inspections is leading to a dramatic increase of defect counts. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. Reduction of inspection costs and increase of throughput is crucial in view of CoO. Detection particles at critical size may not exist. Detection of line edge roughness due to process variation. Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. Filtering and use of Automatic Defect Classification (ADC) is a potential solution for reduction of noise. Reduction of background noise from detection units and samples to improve the sensitivity of systems. Improvement of signal to noise ratio to delineate defect from process variation. Where does process variation stop and defect start?
Wafer edge and bevel control and inspection — Defects and process problems around wafer edge and wafer bevel are identified to cause yield loss.	Find a for production suitable inspection of wafer edge, bevel and apex on the wafer front and backside.
Process stability versus absolute contamination level including the correlation to yield — Test structures, methods, and data are needed for correlating process fluid contamination types and levels to yield and determine required control limits.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect. Definition of maximum process variation (control limits).
Linking systematic yield loss to layout attributes — The irregularity of features makes logic areas very sensitive to Systematic Mechanisms Limited Yield (SMLY) such as patterning marginalities across the lithographic process window.	SMLY should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis run time per die. d) Statistical aggregation of diagnosis results for building a layout-dependent systematic yield model. Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.
High aspect ratio inspection (HARI) — The requirement for high-speed and cost-effective high aspect ratio inspection tools remains as the work around using e-beam inspection does not at all meet requirement for throughput and low cost. Sensitivity requirements are leading to a dramatic increase of defect counts. The major challenge is to find the yield relevant defect types under the vast amount of defects.	Poor transmission of energy into bottom of via and back out to detection system. Rapid detection of defects at ½× Ground Rule (GR) associated with high-aspect-ratio contacts, vias, and trenches, and especially defects near or at the bottoms of these features Large number of contacts and vias per wafer
Difficult Challenges < 22 nm	*Summary of Issues*
In-line defect characterization and analysis — Alternatives to Energy Dispersive X-ray (EDX) analysis systems are required for in-line defect characterization and analysis for defects smaller 100 nm [1]. The focus has to be on light elements, small amount of samples due to particle size following the miniaturization, and microanalysis.	The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. It will be recommended to supply information on chemical state and bonding especially of organics. Small volume technique adapted to the scales of technology generations. Capability to distinguish between the particle and the substrate signal.
Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Development of test structures for new technology generations Address complex integration issues Model ultra-thin film integrity issues Improve scaling methods for front-end processes including increased transistor packing density

[1] Cross-link to Metrology chapter

METROLOGY

WHAT'S NEW?

Metrology is defined as the science of measurement. For the past several years, the ITRS has provided an industry consensus look into the extension of CMOS and the nano-scale technology beyond CMOS. The nanoscale nature of today's transistor and interconnect features results in new materials properties that alter many basic assumptions in measurement and its associated models. The 2007 ITRS Metrology Roadmap discusses the status of key measurements such as critical dimension metrology, overlay, front end and interconnect film and process metrology. It also discusses measurement needs for Emerging Materials and Devices.

The ITRS Metrology TWG found that existing CD metrology methods can be enhanced to extend them to the 32 nm ½ pitch and possibly the 22 nm ½ pitch. Overlay metrology faces new issues if dual patterning and dual exposure processes are quickly moved into manufacturing. Although high k and metal gates have been moved forward into volume manufacturing in 2009, metrology requirements remain process dependent. One key example is nitrogen concentration and profile control in the high k and its interfaces. Stress metrology for process enhanced mobility is explored in greater detail in the 2007 Metrology Roadmap, and the TWG found that the variety of processes used to stress the channel mean a lack of consensus on the best approach. Interconnect Metrology and Frond End Process Metrology both have unmet need of in-line measurement of sidewall film thickness. FinFETs and interconnect trenches are just two examples of structures requiring sidewall metrology. Some future needs for Interconnect Metrology require a coordinated effort including 3D Interconnect and carbon nanotubes metrology.

Gaps in measurement technology require emphasis. Gaps can be found in both CMOS extension and beyond CMOS. *One gap is the ability to measure properties of materials such as thickness on the sidewalls of densely patterned features such as gates, FINS, and trenches.* Another gap is meeting the fundamental challenge for materials characterization of imaging and measurement of materials properties at atomic dimensions. Here, the most often mentioned goal is to provide 3D, atomic resolution measurements. The fact that some materials properties are not localized to atomic dimensions is noteworthy. The fundamental challenge for factory metrology will be the measurement and control of atomic dimensions while maintaining profitable high volume manufacturing.

The Metrology roadmap has repeated the call for a proactive research, development, and supplier base for many years. The relationship between metrology and process technology development needs fundamental restructuring. In the past the challenge has been to develop metrology ahead of target process technology. Today we face major uncertainty from unresolved choices of fundamentally new materials and radically different device designs. *Understanding the interaction between metrology data & information and optimum feed back, feed forward, and real-time process control are key to restructuring the relationship between metrology and process technology.*

A new section has been added to the Metrology Roadmap that covers metrology needs for emerging technology paradigms such as spintronics and molecular electronics. The wide variety of materials and devices described in the Emerging Research Materials and Emerging Research Devices sections provides a challenge to both resources and measurement technology. For example, imaging and measuring soft materials found in molecular electronics is considerably different from the materials used for nanowires, nanotubes, and spintronics. The impact of quantum confinement and quantum size effects as well as surface states alters the optical and electrical properties of materials. A diverse set of measurement needs is described here and in the Emerging Research Materials and Emerging Research Devices sections.

Metrology tool development requires access to new materials and structures if it is to be successful. It requires the availability of state-of-the-art capabilities to be made available for fabrication of necessary standards and development of metrology methodologies in advance of production. This requires a greater attention to expanding close ties between metrology development and process development. When the metrology is well matched to the process tools and processes, ramping times for pilot lines and factories are reduced. An appropriate combination of well-engineered tools and appropriate metrology is necessary to maximize productivity while maintaining acceptable cost of ownership.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 22 nm technology generation. Metrology needs after 2015 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table ITWG14 presents the ten major challenges for metrology.

Table ITWG14 Metrology Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Dual Patterning Lithography, complicated 3D structures such as capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Overlay measurements for Dual Patterning have tighter control requirements. Overlay defines CD. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 22 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for *beyond CMOS.*	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

MODELING AND SIMULATION

WHAT'S NEW?

In 2007, the same approach as in the preceding years has been followed in the Modeling and Simulation chapter:

As a cross-cut chapter it again started from a through analysis of the requirements of the other ITWGs, especially regarding the technological options chosen and the time schedules estimated by them. This resulted both in elaborate crosscut texts with each of these ITWGs and directed the preparation of the 2007 Modeling and Simulation text and tables, which took these requirements on board and complemented them with the assessment of the technical state-of-the-art and possibilities. In turn, the text of the 2007 Modeling and Simulation chapter was rewritten or updated in order to capture these developments, although its structure consisting of ten topical subchapters was left unchanged.

In 2007 there have been two major changes in the Modeling and Simulation Difficult Challenges. Most apparent, two challenges have been replaced: The former short-term challenge "High-frequency device and circuit modeling for 5-100 GHz applications" has been replaced by the new short-term challenge "Circuit element and system modeling for high frequency (up to 160 GHz) applications." The reason for this was that some requirements of that 2005/2006 challenge have in the meantime been met, and on the other hand side the importance of extending simulation up to system level (e.g., SoC, SiP) has strongly increased. Furthermore, the impact of process variations up to circuit level had to be included. These and some other new aspects lead to a considerable shift in scope between the old and the new challenge. Second, the 2005/2006 long-term challenge "Prediction of dispersion of circuit parameters" has been pulled in to short-term, and its various aspects been extended and distributed there across the short-term challenges "Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability" (where variability is now explicitly included), "Ultimate nanoscale device simulation capability," and as already mentioned "Circuit element and system modeling for high frequency (up to 160 GHz) applications." The reason was that the impact of variability and fluctuations has in the meantime developed to a problem to be tackled quickly in order to provide solutions in time for the upcoming technology generations which could be critically effected by these effects. Linked with this, the former short-term challenge on "Lithography simulation including NGL" has been separated into a short-term one "Lithography simulation including EUV" and its long-term counterpart "NGL simulation," which deals with the favorite non-optical and non-EUV techniques. Besides this, some updates were implemented on several other challenges, and the short-term challenges were put in a logical order which starts with lithography simulation and extends until circuit element and system modeling, without prioritizing among these six challenges.

The development of the technological capabilities and the requirements of the focus ITWGs, especially PIDS, FEP, Lithography and interconnect have resulted in many changes in the details of the Modeling and Simulation requirements, see the respective tables. Furthermore, during the preparation of these tables several topics where identified where results were already requested for 2005 or 2006, but sufficient research could not be carried out around the world due to lack of resources. In turn, were still needed these topics again show up in the current requirement tables. Concerning the main research areas requested, for Front End Process Modeling both continuum diffusion and activation models on one hand side and atomistic modeling for activation and diffusion on the other hand side are now separate main items, where etching and deposition has been combined into one line. The requirements for the modeling of novel devices have been extended beyond memories. Large area lithography simulation now includes TCAD-based inverse lithography modeling.

The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry, along the simulation food chain mentioned above. Because the necessary basic work generally needs significant development time, it is vital that adequate research funds will be made available in a timely manner in order to address the industry's future critical needs.

DIFFICULT CHALLENGES

The difficult challenges highlighted in Table ITWG15 are those Modeling and Simulation requirements which on one hand must be met in time to support the high-level progress of the roadmap and on the other hand are most critical to fulfill due to their technical difficulty and the R&D resources needed. Additionally, it should be noted that a key difficult challenge present across all the modeling areas is that of experimental validation. This challenge is especially difficult because for most processes many physical effects interact with each other and must be appropriately separated by well-selected experiments, in order to be able to develop predictive models and not simply fit experimental data. As devices shrink and new materials are introduced into the technology arena, new and enhanced analytical techniques are vital that can extract the necessary information for this model development and evaluation validation from the experiments. This critical need is mentioned as a cross-cut item with the Metrology ITWG.

Table ITWG15 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Lithography simulation including EUV	Experimental verification and simulation of ultra-high NA vector models, including polarization effects from the mask and the imaging system
	Models and experimental verification of non-optical immersion lithography effects (e.g., topography and change of refractive index distribution)
	Simulation of multiple exposure/patterning
	Multi-generation lithography system models
	Simulation of defect influences/defect printing
	Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography
	Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects and ultra-high NA effects (oblique illumination)
	Predictive resist models (e.g., mesoscale models) including line-edge roughness, etch resistance, adhesion, mechanical stability, and time-dependent effects in multiple exposure
	Resist model parameter calibration methodology (including kinetic and transport parameters)
	Simulation of ebeam mask making
	Simulation of directed self-assembly of sublithography patterns
	Modeling lifetime effects of equipment and masks
Front-end process modeling for nanometer structures	Diffusion/activation/damage/stress models and parameters including SPER and millisecond processes in Si-based substrate, that is, Si, SiGe:C, Ge, SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers Modeling of epitaxially grown layers: Shape, morphology, stress Modeling of stress memorization (SMT) during process sequences Characterization tools/methodologies for ultra shallow geometries/junctions, 2D low dopant level, and stress Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces Efficient and robust 3D meshing for moving boundaries Front-end processing impact on reliability
Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-)products, rates ...), and simplified but physical models for complex chemistry and plasma reaction Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction) Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects) Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling Efficient extraction of impact of equipment- and/or process induced variations on devices and circuits, using process and device simulation
Ultimate nanoscale device simulation capability	Methods, models and algorithms that contribute to prediction of CMOS limits General, accurate, computationally efficient and robust quantum based simulators including fundamental parameters linked to electronic band structure and phonon spectra Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS Models (including material models) to investigate new memory devices like MRAM, PRAM, etc. Gate stack models for ultra-thin dielectrics Models for device impact of statistical fluctuations in structures and dopant distribution Efficient device simulation models for statistical fluctuations of structure and dopant variations and efficient use of numerical device simulation to assess the impact of variations on statistics of device performance Physical models for novel materials, e.g., high-k stacks, Ge and compound III/V channels …: Morphology, band structure, defects/traps... Reliability modeling for ultimate CMOS Physical models for stress induced device performance

Table ITWG15 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical, thermodynamic and electronic properties of low κ, high κ, and conductors for efficient on-chip and off-chip including SIP layout and power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension Model effects which influence reliability of interconnects/packages including 3D integration (e.g., stress voiding, electromigration, fracture, piezoelectric effects) Models to predict adhesion on interconnect-relevant interfaces Simulation of adhesion and fracture toughness characteristics for packaging and die interfaces Models for electron transport in ultra fine patterned interconnects
Circuit element and system modeling for high frequency (up to 160 GHz) applications	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies and package: - possibly consisting of different technologies, - covering and combining different modeling and simulation levels as well as different simulation domains Scalable active component circuit models including non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling Scalable passive component models for compact circuit simulation, including interconnect, transmission lines, RF MEMS switches, … Physical circuit element models for III/V devices Computer-efficient inclusion of variability including its statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently Efficient building block/circuit-level assessment using process/device/circuit simulation, including process variations
Difficult Challenges < 22 nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Gate stacks: Predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. 2) Models for novel integrations in 3D interconnects including airgaps and data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. Modeling-assisted metrology. 4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices including Emerging Research Materials	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), quantum dots, molecular electronics, multiferroic materials and structures, strongly correlated electron materials) Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …)
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling. Physical design tools for integrated electrical/optical systems
NGL simulation	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects and impact on LER); heating and charging effects), including impact on device characteristics (e.g., due to local crystal damage by electron scattering or charging effects) Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) tables are created early in the Roadmap process and are used as the basis for initiating the activities of the International Technology Working Groups in producing their detailed chapters. These tables are also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the TWGs by highlighting inconsistencies between the specific tables. The process to revise the tables includes increasing levels of cross-TWG and international coordination and consensus building to develop underlying models of trends and to reach agreement on target metrics. As a result, the ORTC tables undergo several iterations and reviews.

The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group chapter. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update and renewal work that began in 2006. Additionally, the ORTC Glossary has been updated in 2007.

OVERVIEW OF 2007 REVISIONS

DEFINITIONS

As noted above, the Overall Roadmap Technology Characteristics tables provide a consolidated summary of the key technology metrics. Please note that, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds 10,000 units per month of ICs from a manufacturing site using “production tooling.” Furthermore, a second company must begin production within three months (see Figure 2). To satisfy this timing definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

It was mentioned in the Introduction section of the ITRS Executive Summary, but it is worth repeating, that there continues to be confusion in the industry regarding individual company public press announcements of their “node” progress and timing, which may or may not align with the ITRS definitions and specific targets.

During the 2003 ITRS development, an attempt was made to reconcile the many published press releases by Logic manufacturers referencing “90 nm” technology “node” manufacturing in 2003. Since the contacted metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM stagger-contacted M1 half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that some of the public citations were in reference to an “indexed” technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance). Some companies also referenced the timing for doubling of functionality on a given product (for example the doubling of logic gates or memory bits) as a measure of “node” advancement. This approach of measuring technology progress complicates the “node” relationship, because density improvements can be accomplished by design improvements added along with linear lithographic feature size reduction.

Additional confusion has developed due to the technology “node” references in Flash memory product announcements, and Flash technology is receiving increased emphasis in both the 2005 and 2007 ITRS. For example, Flash product cell density is defined by the un-contacted poly-silicon (poly) interconnect half-pitch, rather than a metal 1 (M1) half-pitch (the key feature which drives density in DRAM and MPU and ASIC products). Also, very aggressive Flash memory Cell Area Factor (see Glossary) improvements have been added by Flash cell designers in order to aggressively reduce costs and meet the rapidly ramping demand for non-volatile memory (NVM) storage.

The International Roadmap Committee (IRC) decided in the 2007 ITRS roadmap that the best way to minimize confusion between the ITRS and individual company public announcements is to continue the separate tracking of the various technology trend drivers by product—DRAM, MPU/ASIC, and Flash. As mentioned earlier, the MPU/ASIC and DRAM product half-pitches are now both defined by a common reference to the M1 stagger-contact, while the Flash NVM

product is referenced to un-contacted poly dense parallel lines (refer to Figure 1). Individual TWG tables will utilize the product table header line items that are most representative of the technology trend drivers for each table.

Due to the new emphasis on separate product trend tracking, no common product technology header is required – only the year of production of the referenced technology line item. In the 2007 ITRS, the technology trends and the functional (transistors, bits, logic gates) or characteristic (speed, power) performance associated with the individual product groups (DRAM, Flash, MPU, ASIC) will be emphasized. Individual company references that wish to compare to the ITRS must now reference the specific product technology trend line item, as further defined by the ITRS Executive Summary and Glossary.

Individual product technology trends continue to be monitored, and the most recent TWG survey update is indicating that the DRAM historical trend may be tracking closer to the ITRS MPU trend. However, the 2007 DRAM M1 half-pitch targets were left unchanged in the 2007 ORTC Tables. The DRAM trends and M1 targets will be investigated further in 2007 and reported in the 2008 Update, but additional details from the latest survey are included in the 2007 PIDS chapter. Some minor inconsistencies may appear in the 2007 and 2008 years, and the 2007 ITRS targets for those years are may be slightly more aggressive than actual industry performance. All targets from 2009 and beyond, the timing which influences the Grand Challenges and Potential Research and Development solutions are consistent with the latest survey results.

In the most recent Flash technology survey, the overall lithography resolution now appears to be driven at the most leading edge by a feature size trend from Flash product. For example, as is described in additional detail below, the uncontacted polysilicon half-pitch of FLASH memories is now projected to be ahead of DRAM stagger-contacted M1 half-pitch by two years by 2008. A two-year lead by the Flash uncontacted polysilicon half-pitch is considered equivalent (in lithographic processing difficulty) to a one-year lead of the DRAM stagger-contacted M1 half-pitch, and this additional timing lead increase is therefore causing Flash memory technology to drive leading-edge lithography. Please see the Glossary section for additional detail on the "Year of Production" timing definition.

The 2007 ITRS table technology trend targets have now been completely annualized from 2007 through the 15-year Roadmap horizon in 2022. However, per previously established IRC guidelines, the 2007 ITRS retains the definition of a technology trend cycle time as the period of time to achieve a significant advancement in the process technology. To be explicit, a technology trend cycle time advancement continues to be defined as the period of time to achieve an approximate 0.71× reduction per cycle (precisely 0.50× per two cycles). Refer to Figures 5 and 6.

Please note from the 2007 ITRS ORTC Table 1a and 1b, that the timing of a technology cycle remains different for a particular product. For example, the DRAM stagger-contact half-pitch M1 in the 2007 ITRS is still forecast to be on a 0.71×/3-years (0.50×/6-years) timing cycle from the historical 2004/90 nm actual (after being on a two-year timing cycle pace from the 2000/180 nm actual through 2004/90nm). The DRAM 3-year cycle is presently forecast to continue on a 3-year cycle through the 2022/11 nm target. The annual multiplier for the three-year cycle timing is 0.8909×/year, which is used to calculate the interim annual trend targets (examples: 2009/50 nm, 2020/14 nm).

After taking into account the available industry data and ITWG and IRC inputs, consensus was reached on the new Flash product technology timing model, based on the uncontacted polysilicon half-pitch definition. The Flash uncontacted polysilicon half-pitch is now set on a two-year cycle timing pace from 2000/180 nm through 2008/45 nm. At this point, it was determined by the Lithography ITWG that the Flash uncontacted polysilicon half-pitch, numerically two years "ahead" of the DRAM stagger-contacted M1 half-pitch, is now driving the technology process equipment being used to achieve that target. After 2008/45 nm, the Flash uncontacted polysilicon half-pitch is expected to turn to a three-year timing cycle, two years ahead of the DRAM trend, and would extend to 2022/9 nm on an annual basis.

As noted above, the MPU (and high-performance ASIC) Product Trend cycle timing was changed in the 2005 ITRS to be based on the same stagger-contact M1 half-pitch definition as DRAM. After analysis of historical data and consensus agreement by the ITWGs and IRC, the MPU M1 half-pitch was set on a 2.5-years (0.50×/5-years) cycle timing pace from the historical 2000/180 nm actual point through 2010/45 nm. At the 2010/45 nm point, it was decided that the MPU M1 targets would "catch up" and become equal to the DRAM M1 cycle timing targets (3-year timing cycle) through the end of the roadmap in 2022.

The MPU (and high-performance ASIC) final physical gate-length (phGL) targets remain unchanged from the 2003 ITRS, in which the timing was set at a two-year cycle (0.5×/4-years; 0.8409×/year) from 1999 through the 2005/32 nm point, and then the trend targets revert to a three-year timing (0.5×/6 years; 0.8909/year) cycle through the end of the Roadmap to 2022/4.5 nm. The Lithography and FEP ITWGs continue with their agreement on a new ratio (1.6818× multiplier above the physical gate length) between the final physical gate length, which includes etch, and the printed gate length targets.

The low-operating-power ASIC gate length targets were established by the PIDs ITWG, and were placed two years behind the MPU (and high-performance ASIC) printed gate length and physical gate length targets.

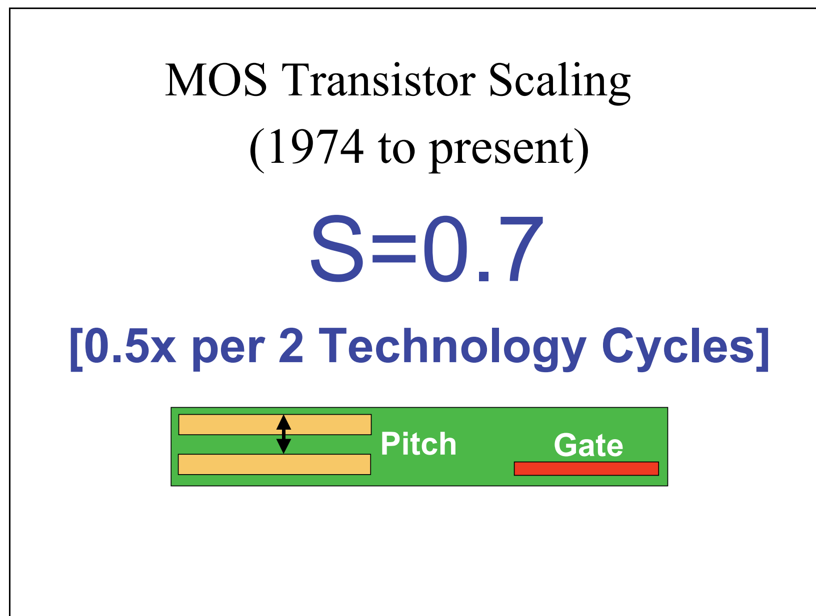

Figure 5 MOS Transistor Scaling—1974 to present

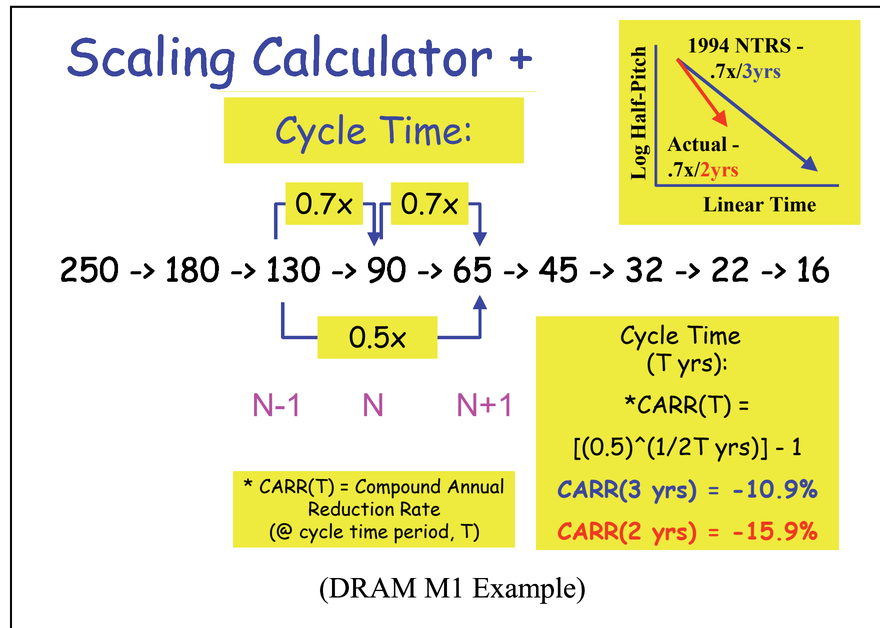

Figure 6 Scaling Calculator

ROADMAP TIMELINE

The 2007 edition of the Roadmap maintains a 15-year projection, from 2007 as a reference year and through 2022. The timing trends of the future technology pace of the DRAM product still represents the leading edge for stagger-contacted M1 half-pitch, and is forecast to return to the three-year cycle (three years between 0.71× reduction of the feature size)

after 90nm/2004, unchanged from the 2003 edition. From surveys updates by the PIDS TWG, the 90 nm DRAM half-pitch began production ramp in 2004, on the completion of customer product qualification, which was made an explicit requirement of the "Production" definition for DRAM product for the 2003 ITRS.

In the 2001 ITRS, the 130 nm DRAM product M1 half-pitch was pulled in an additional year (from 2002 in the 1999 ITRS to 2001), anticipating a continuation of an observed historical two-year technology cycle calculated from 350 nm/1995, 250 nm in 1997, 180 nm in 1999). Data provided by DRAM manufacturers in 2003, which was based upon the more rigorous customer-product-qualified production ramp, indicated that the actual production ramp timing was as follows: 350 nm/1995, 250 nm/1998, 180 nm/2000 and 130 nm/2002. This new data indicates a two-year cycle timing, but delayed one year from the original 2001 ITRS timing. Data gathered on actual DRAM product ramped in the 2004 PIDS member surveys confirmed the two-year cycle step between 130 nm/2002 and 90 nm/2004. Although there was the possibility of a continuation of this new delayed two-year cycle trend, the 2004 DRAM product manufacturer consensus, confirmed by the PIDS 2004 survey update, continued to project a three-year timing cycle (0.71× reduction) for DRAM stagger-contacted M1 half-pitch throughout the 2007–2022 Roadmap period, as illustrated in Figure 7. As mentioned above, the most recent PIDS DRAM survey work has indicated that DRAM technology pace may be relaxed to be closer to the MPU M1 half-pitch 2.5-year cycle numbers. These survey recommendations will be continue to be evaluated for revision of the 2008 ITRS Update tables.

Also mentioned above, the DRAM interconnect half-pitch will no longer continue to be used as a representative feature of leading-edge semiconductor manufacturing technology for defining the achievement of a technology cycle (0.71× reduction of the feature size). In fact, the Flash uncontacted polysilicon half-pitch feature is now acknowledged as leading the DRAM M1 targets numerically by two years, and now is now the most leading driver of leading-edge technology manufacturing. Similarly, as mentioned, the lagging MPU and ASIC M1 stagger-contacted M1 interconnect half-pitches are running at a faster 2.5-year cycle pace and are presently expected to catch up and remain equal to the DRAM half-pitch in 2010/45 nm. With the new product-oriented focus since the 2005 ITRS, all product technology trends will be monitored, and any of the product trends may accelerate further and begin to drive the industry research and the equipment and materials supplier development at the leading edge. See Figure 7.

ROUNDED TREND NUMBERS

Using 180 nm DRAM product half pitch in the year 2000 as the calculation standard for trends, the 2007 ITRS now includes a correction of the past "rounding" convention for the technology cycle trend target. The actual calculated mathematical trend data (used for model calculations in the ORTC and TWG tables) reduces by 50% every other technology cycle, resulting in actual versus rounded number targets comparison below, starting from 350 nm in 1995, as follows in Table C.

Table C Rounded versus Actual Trend Numbers (DRAM Product Trend Example)

YEAR OF PRODUCTION	*1995*	*1998*	*2000*	*2002*	*2003*	*2004*	*2006*	*2007*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*	*2019*	*2022*
Calculated Trend Numbers (nm)	**360**	**255**	**180**	**127.3**	**101**	**90**	**71.4**	**63.6**	**50.5**	**45**	**35.7**	**31.8**	**25.3**	**22.5**	**17.9**	**15.9**	**11.3**
ITRS Rounded Numbers (nm)	**350**	**250**	**180**	**130**	**100**	**90**	**70**	**65**	**50**	**45**	**36**	**32**	**25**	**22**	**18**	**16**	**11**

Note the new rounding corrections become more critical as the industry moves into the two-digit data cycles of the new nanotechnology (sub-100 nm) era. Please note also that some regions, for their own legacy publication consistency, will retain their right to continue to track the previous technology generations beginning with 100 nm/2003. Starting from 100 nm in 2003 will result in "milestones" that are targeted one year earlier than the present 2003 roadmap convention (example: 70 nm/2006; 50 nm/2009; 36 nm/2012; 25 nm/2015, etc.). By consensus of the IRC both number sets are available for long-term calculations, since the original 2001 ITRS long-term columns were retained (2010/45 nm; 2013/32 nm; 2016/22 nm), and new columns (2012/36 nm; 2015/25 nm; 2018/18 nm; 2021/13 nm) are now annualized and included as columns.

UPDATES TO THE ORTC

The MPU/ASIC M1 half-pitch continues to be defined as a stagger-contacted half-pitch the same as DRAM and both remain unchanged from the 2005 ITRS. , The Flash product half-pitch continues to be defined as an uncontacted

polysilicon half-pitch, and has been revised from the 2005 ITRS by continuing the 2-year cycle trend through 2008/45 nm, then turning to a 3-year cycle through 2022..The *printed* MPU gate length received a major correction to more an aggressive starting point in the 2001 ITRS. In addition, a new *physical* gate length is being tracked that further reduces the bottom gate length dimension of a fully processed transistor. The physical gate length trends remain unchanged for the 2003 through the present 2007 ITRS, and are now forecast to continue scaling on a three-year cycle basis through the Roadmap horizon in 2022,. Refer to Figure 7.

The ORTC metrics are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to secure industry leadership. Thus, the highly competitive environment of the semiconductor industry quickly tends to make obsolete many portions of the ORTC metrics and, consequently, the Roadmap. Hopefully, the gathering and analysis of actual data, combined with the ITRS annual update process will provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS to the industry.

For example, the actual data and conference papers, along with company survey data and public announcements will be re-evaluated during the year 2008 ITRS Update process, and the possibility of a continued two-year node cycle in some of the individual product technology trends. As mentioned above, to reflect the variety of cycles and to allow for closer monitoring of future Roadmap trend shifts, it was agreed to continue the practice of publishing annual technology requirements from 2007 through 2015, called the “Near-term Years,” and also annual requirements from 2015 through 2022, called the “Long-term years.”

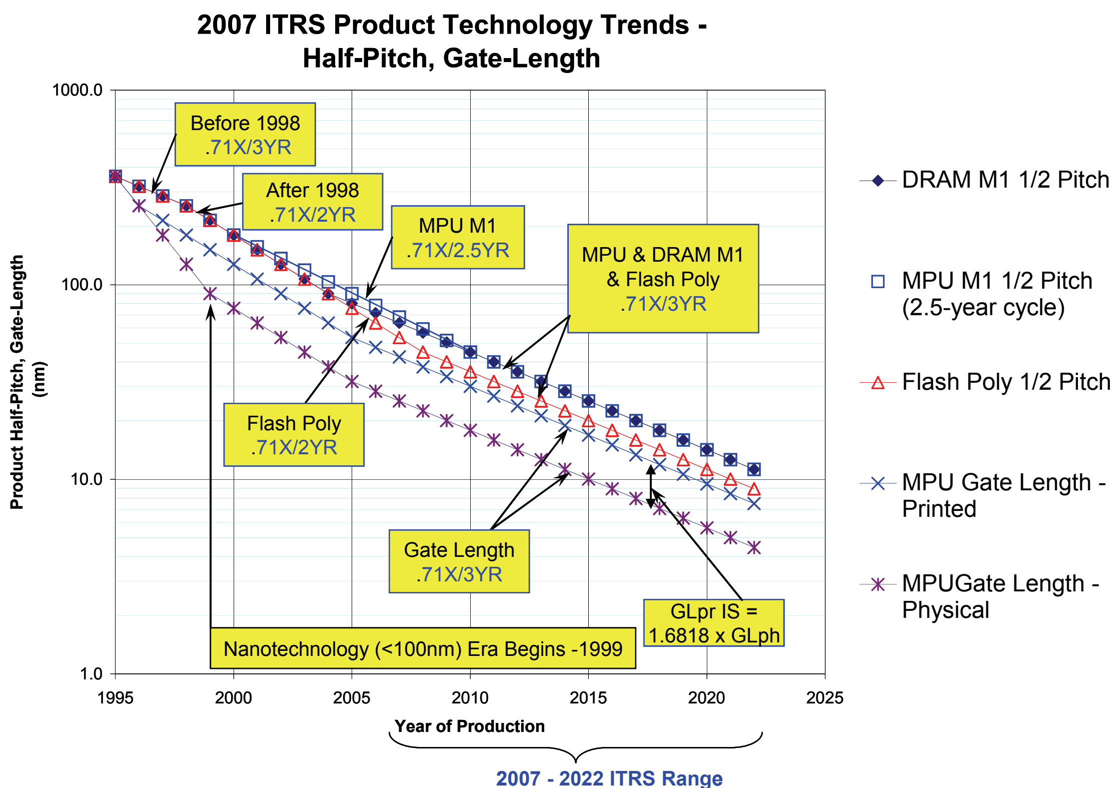

Figure 7 2007 ITRS—Half Pitch and Gate Length Trends

PRODUCT GENERATIONS AND CHIP-SIZE MODEL

This section discusses "product generations" and their relationship to technology cycles, since, in the past, these terms have often been used interchangeably. However, the historically simple picture of a new DRAM product generation every three years (at 4× the previous density and based on an essentially new set of technology features) has become obsolete as a way to define technology cycle timing advancement. Continuing a practice that began with the 2005 ITRS, the 2007 ITRS edition bases the technology pace drivers on individual product technology trends. These product-based technology trends may move on different paces from one another, based upon market functionality and performance and affordability needs, as the leading-edge product evolution/shrink paths becomes more complex.

Historically, DRAM products have been recognized as the technology drivers for the entire semiconductor industry. Prior to the late-1990s, logic (as exemplified by MPU) technology moved at the same pace as DRAM technology, but after 2000/180 nm began moving at a slower 2.5-year technology cycle pace, while DRAM technology continued on the accelerated two-year pace. During the last few years, the development rate of new technologies used to manufacture microprocessors has continued on the 2.5-year pace, while DRAMs are now forecast to slow to a three-year cycle pace through the 2020 Roadmap horizon. By moving on the faster 2.5-year cycle pace, microprocessor products are closing the half-pitch technology gap with DRAM, and are now also driving the most leading-edge lithography tools and processes—especially for the capability to process the isolated-line feature of the printed and physical gate length. As noted above, the Flash technology, as defined by uncontacted polysilicon, has also accelerated to the point where it is now driving at the most leading edge.

However, several fundamental differences exist between the families of products. Due to strong commodity market economic pressure to reduce cost and increase fab output productivity, DRAM product emphasizes the minimization of the chip size. Therefore, development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. However, this pressure to minimize cell size is in conflict with the requirement to maximize the capacitance of the cell for charge storage performance, which puts pressure on memory cell designers to find creative ways through design and materials to meet minimum capacitance requirements while reducing cell size. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch.

Microprocessors have also come under strong market pressure to reduce costs while maximizing performance. Performance is enabled primarily by the length of the transistor gate and by the number of interconnect layers. The 2007 ITRS teams have reached consensus on models for the required functionality, chip size, cell area, and density for the ORTC tables. The MPU product chip size tables continue to be similar to the DRAM model, with large introductory chip sizes that must shrink over time to achieve the affordable sizes. Additional line items communicate the model consensus, and the underlying model assumptions are included in the ORTC table notations.

Table 1a and 1b summarize the near and long-term technology trend metrics summarized above. For completeness, the ASIC/low power gate length trends are also included, and lag behind the leading-edge MPU in order to maximize standby and operating current drain. See the Glossary section for additional detail on the definition of the half-pitch and gate-length features. For each product generation, both the leading-edge ("at introduction") and the high-volume ("at production") DRAM products are included.

To summarize Figure 7, it should be noted that the long-term average annualized reduction rate of the DRAM contacted M1 half-pitch feature size is forecast to return to the three-year technology cycle pace after 2004/90 nm, which represents an approximately 11%/year (~30% reduction/three years). The previous (1998/250 nm–2004/90 nm) accelerated two-year cycle rate is approximately 16%/year reduction on an annual basis (~30% reduction/two years). As noted above the new Flash memory uncontacted polysilicon turns to the three-year pace in 2008 after crossing over the DRAM M1, and the MPU/ASIC M1 (generically referred to as MPU in graphs) catches up to DRAM M1 in 2010/45 nm, and returns to a three-year pace.

Table 1a Product Generations and Chip Size Model Technology Trend Targets—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Printed Gate Length (nm) ††	42	38	34	30	27	24	21	19	17
MPU Physical Gate Length (nm)	25	23	20	18	16	14	13	11	10
ASIC/Low Operating Power Printed Gate Length (nm) ††	54	48	42	38	34	30	27	24	21
ASIC/Low Operating Power Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
Flash ½ Pitch (nm) (un-contacted Poly)(f)	54	45	40	36	32	28	25	22	20

Table 1b Product Generations and Chip Size Model Technology Trend Targets—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Printed Gate Length (nm) ††	15	13	12	11	9	8.4	7.5
MPU Physical Gate Length (nm)	9	8	7	6.3	5.6	5.0	4.5
ASIC/Low Operating Power Printed Gate Length (nm) ††	19	17	15	13	12	11	9
ASIC/Low Operating Power Physical Gate Length (nm)	11	10	9	8	7	6.3	5.6
Flash ½ Pitch (nm) (un-contacted Poly)(f)	18	16	14	13	11	10	9

Notes for Tables 1a and 1b:

†† MPU and ASIC gate-length (in resist) targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "physical" gate lengths may be reduced from the "as-printed" dimension. These physical gate-length targets are driven by the need for maximum speed performance in logic microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design chapter tables as needs that drive device design and process technology requirements.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

MPU Physical Gate Length targets are unchanged from the 2003 ITRS through the 2006 ITRS Update, but also included are the complete set of annualized Long-term targets through 2022. The printed gate length has been adjusted to reflect the agreement between the FEP and Lithography TWGs to use a standard factor, 1.6818, to model the relationship between the final physical gate length and the printed gate length, after additional processing is applied to that isolated feature.

MPU/ASIC M1 stagger-contact targets was accelerated to 90 nm in 2005 to reflect actual industry performance per the Interconnect ITWG recommendation, and a new consensus model technology cycle timing of 2.5 years (to 0.71× reduction) was applied through 2010, when the trend targets become equal to the DRAM stagger-contact M1 through 2022.

Numbers in the header are rounded from the actual trend numbers used for calculation of models in ITRS ORTC and ITWG tables (see discussion in the Executive Summary on rounding practices).

Table 1c DRAM and Flash Production Product Generations and Chip Size Model—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
DRAM Product Table									
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af2] (um^2)	**0.024**	**0.019**	**0.015**	**0.012**	**0.0096**	**0.0077**	**0.0061**	**0.0048**	**0.0038**
Cell array area at production (% of chip size) §	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**
Generation at production §	**2G**	**2G**	**2G**	**4G**	**4G**	**4G**	**8G**	**8G**	**8G**
Functions per chip (Gbits)	**2.15**	**2.15**	**2.15**	**4.29**	**4.29**	**4.29**	**8.59**	**8.59**	**8.59**
Chip size at production (mm^2)§	**93**	**74**	**59**	**93**	**74**	**59**	**93**	**74**	**59**
Gbits/cm2 at production §	**2.31**	**2.91**	**3.66**	**4.62**	**5.82**	**7.33**	**9.23**	**11.63**	**14.65**
Flash Product Table									
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**53.5**	**45.0**	**40.1**	**35.7**	**31.8**	**28.3**	**25.3**	**22.5**	**20.0**
Cell area factor [a]	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Cell area [Ca = af^2] (um^2)	**0.0115**	**0.0081**	**0.0064**	**0.0051**	**0.0041**	**0.0032**	**0.0026**	**0.0020**	**0.0016**
Cell array area at production (% of chip size) §	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**
Generation at production § SLC	**8G**	**8G**	**8G**	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**
Generation at production § MLC [2 bits/cell]	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**	**64G**	**64G**	**64G**
Generation at production § MLC [4 bits/cell]	**32G**	**32G**	**32G**	**64G**	**64G**	**64G**	**128G**	**128G**	**128G**
Functions per chip (Gbits) SLC	**8.59**	**8.59**	**8.59**	**17.18**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**
Functions per chip (Gbits) MLC [2 bits/cell]	**17.18**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**	**68.72**	**68.72**	**68.72**
Functions per chip (Gbits) MLC [4 bits/cell]	**34.36**	**34.36**	**34.36**	**68.72**	**68.72**	**68.72**	**137.44**	**137.44**	**137.44**
Chip size at production (mm^2)§ SLC	**143.96**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**
Chip size at production (mm2)§ MLC [2 bits/cell & 4 bits/cell]	**143.96**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**
***Bits**/cm^2 at production § SLC*	**5.97E+09**	**8.44E+09**	**1.06E+10**	**1.34E+10**	**1.69E+10**	**2.13E+10**	**2.68E+10**	**3.38E+10**	**4.25E+10**
Bits/cm2 at production § MLC [2 bits/cell]	**1.19E+10**	**1.69E+10**	**2.13E+10**	**2.68E+10**	**3.38E+10**	**4.25E+10**	**5.36E+10**	**6.75E+10**	**8.51E+10**
Functions per chip (Gbits) MLC [4 bits/cell]	**2.39E+10**	**3.38E+10**	**4.25E+10**	**5.36E+10**	**6.75E+10**	**8.51E+10**	**1.07E+11**	**1.35E+11**	**1.70E+11**

Table 1d DRAM and Flash Production Product Generations and Chip Size Model—Long-term Years

Year of Production	2016	2017	2018	2019	2020	2021	2022
DRAM ½ Pitch (nm) (contacted)	22	20	18	16	14	13	11
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	22	20	18	16	14	13	11
MPU Physical Gate Length (nm)	9	8	7	6.3	5.6	5.0	4.5
DRAM Product Table							
Cell area factor [a]	6	6	6	6	6	6	6
Cell area [Ca = af2] (um^2)	0.0030	0.0024	0.0019	0.0015	0.0012	0.00096	0.00076
Cell array area at production (% of chip size) §	56.08%	56.08%	56.08%	56.08%	56.08%	56.08%	56.08%
Generation at production §	16G	16G	16G	32G	32G	32G	64G
Functions per chip (Gbits)	17.18	17.18	17.18	34.36	34.36	34.36	68.72
Chip size at production (mm^2)§	93	74	59	93	74	59	93
Gbits/cm2 at production §	18.46	23.26	29.31	36.93	46.52	58.61	73.85
Flash Product Table							
Flash ½ Pitch (nm) (un-contacted Poly)(f)	17.9	15.9	14.2	12.6	11.3	10.0	8.9
Cell area factor [a]	4	4	4	4	4	4	4
Cell area [$Ca = af^2$] (um^2)	0.0013	0.0010	0.00080	0.00064	0.00051	0.00040	0.00032
Cell array area at production (% of chip size) §	68.35%	68.35%	68.35%	68.35%	68.35%	68.35%	68.35%
Generation at production § SLC	64G	64G	64G	128G	128G	128G	256G
Generation at production § MLC [2 bits/cell]	128G	128G	128G	256G	256G	256G	512G
Generation at production § MLC [4 bits/cell]	256G	256G	256G	512G	512G	512G	1024G
Functions per chip (Gbits) SLC	68.72	68.72	68.72	137.44	137.44	137.44	274.88
Functions per chip (Gbits) MLC [2 bits/cell]	137.44	137.44	137.44	274.88	274.88	274.88	549.76
Functions per chip (Gbits) MLC [4 bits/cell]	274.88	274.88	274.88	549.76	549.76	549.76	1099.51
Chip size at production (mm^2)§ SLC	128.26	101.80	80.80	128.26	101.80	80.80	128.26
Chip size at production (mm2)§ MLC [2 bits/cell & 4 bits/cell]	128.26	101.80	80.80	128.26	101.80	80.80	128.26
Bits/cm^2 at production § SLC	5.36E+10	6.75E+10	8.51E+10	1.07E+11	1.35E+11	1.70E+11	2.14E+11
Bits/cm2 at production § MLC [2 bits/cell]	1.07E+11	1.35E+11	1.70E+11	2.14E+11	2.70E+11	3.40E+11	4.29E+11
Functions per chip (Gbits) MLC [4 bits/cell]	2.14E+11	2.70E+11	3.40E+11	4.29E+11	5.40E+11	6.80E+11	8.57E+11

Notes for Tables 1c and 1d:

§ DRAM Model—cell area factor (design/process improvement) targets are as follows:

1999–2006/8×: 2006-2022/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the last model 2005 ITRS timeframe refer to Figures 8 and 9 for bit size and bits/chip trends:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the latest DRAM consensus model changes for the 2007 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM product are delayed an additional year and now remains "flat" at less than 93 mm^2, about one third smaller than the MPU model. However, with the pull-in of the $6f^2$ "cell area factor" , the flat-chip-size model target still requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c, 1d).

In addition to the revisions noted above, the cell array efficiency (CAE – the Array % of total chip area) was change to 56.1% after 2006. Only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery, however, the CAE pull-in enables the production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

The Flash product model was also revised to extend the 2-year-cycle half-pitch to 2008, also targets an affordable (<145 mm^2) chip size and includes a doubling of functions (bits) per chip every technology cycle (three years after 2008) on an Inter-generation. Flash cells have reached a limit of the 4-design factor, so the reduction of the Flash single-level cell (SLC) size is paced by the uncontacted polysilicon (three-year cycle). However, the Flash technology has the ability to store and electrically access two bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half the size of an SLC product cell size; and the latest revision of the Flash model also includes the introduction of 4 bits/cell beginning 2010 (refer to Figures 8 and 9).

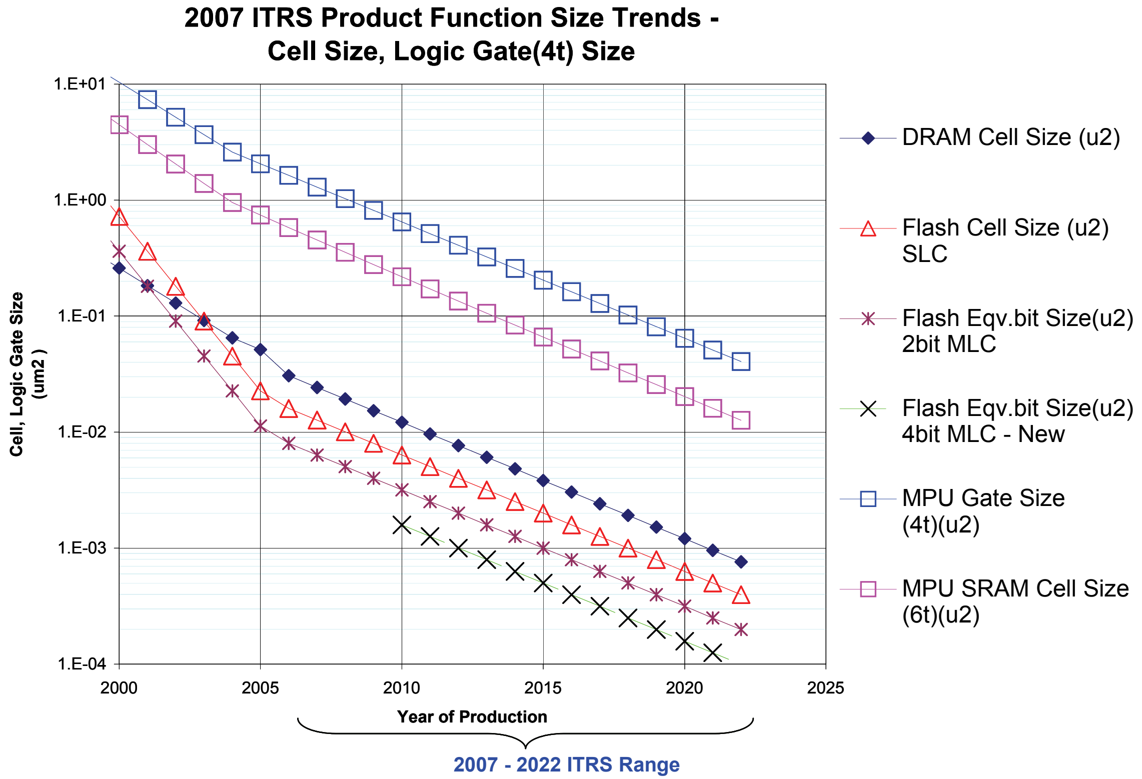

Figure 8 2007 ITRS Product Function Size Trends:
MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]

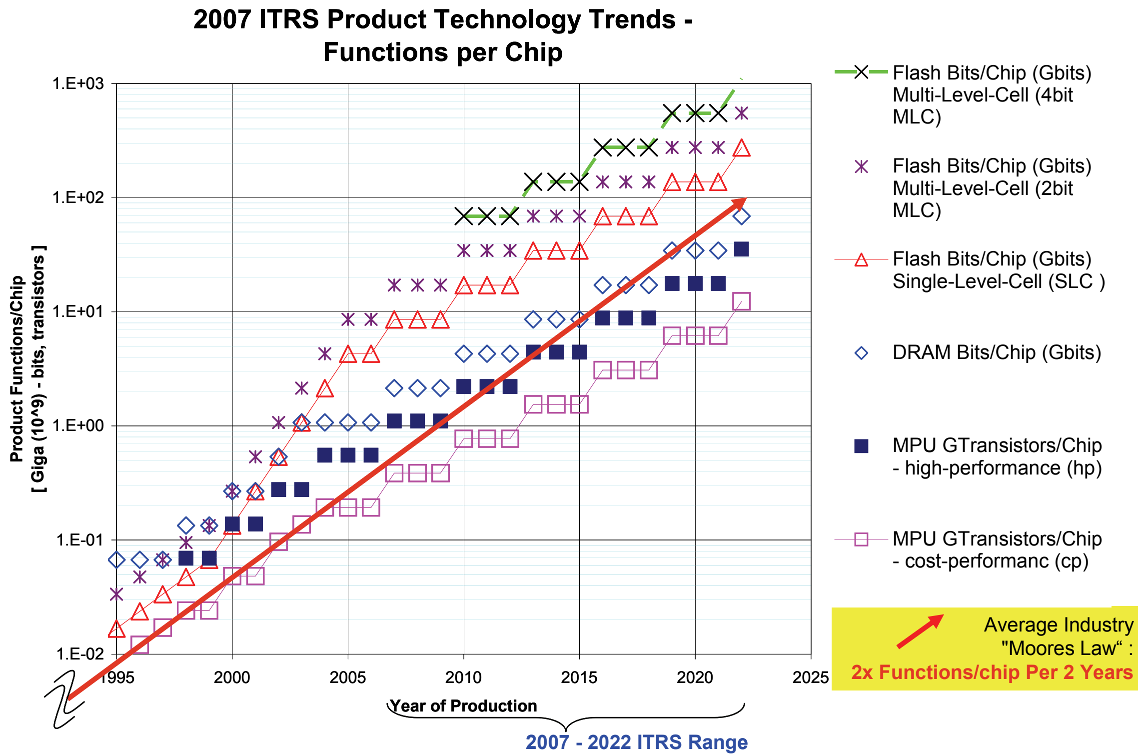

Figure 9 2007 ITRS Product Technology Trends:
Product Functions/Chip and Industry Average "Moore's Law" Trends

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af^2] (um^2)	**0.024**	**0.019**	**0.015**	**0.012**	**0.0096**	**0.0077**	**0.0061**	**0.0048**	**0.0038**
Cell array area at introduction (% of chip size) §	**73.52%**	**73.76%**	**73.97%**	**74.16%**	**74.30%**	**74.47%**	**74.61%**	**74.70%**	**74.83%**
Generation at introduction §	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**	**64G**	**64G**	**64G**
Functions per chip (Gbits)	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**	**68.72**	**68.72**	**68.72**	**68.72**
Chip size at introduction (mm^2) §	**568**	**449**	**711**	**563**	**446**	**706**	**560**	**444**	**351**
Gbits/cm^2 at introduction §	**3.03**	**3.82**	**4.83**	**6.10**	**7.70**	**9.73**	**12.28**	**15.49**	**19.55**

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af^2] (um^2)	**0.0030**	**0.0024**	**0.0019**	**0.0015**	**0.0012**	**0.00096**	**0.00076**
Cell array area at introduction (% of chip size) §	**74.93%**	**75.00%**	**75.09%**	**75.18%**	**75.27%**	**75.36%**	**75.45%**
Generation at introduction §	**128G**	**128G**	**128G**	**256G**	**256G**	**256G**	**512G**
Functions per chip (Gbits)	**137.44**	**137.44**	**137.44**	**274.88**	**274.88**	**274.88**	**549.76**
Chip size at introduction (mm^2) §	**557**	**442**	**350**	**555**	**440**	**349**	**553**
Gbits/cm^2 at introduction §	**24.67**	**31.11**	**39.24**	**49.50**	**62.44**	**78.77**	**99.36**

Notes for Tables 1e and 1f:

§ DRAM Model—cell area factor (design/process improvement) targets are as follows:

1999–2006/8×: 2006-2022/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the last model 2005 ITRS timeframe refer to Figures 8 and 9 for bit size and bits/chip trends:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the latest DRAM consensus model changes for the 2007 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM product are delayed an additional year and now remains "flat" at less than 93 mm^2, about one third smaller than the MPU model. However, with the pull-in of the 6f^2 "cell area factor" , the flat-chip-size model target still requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c, 1d).

In addition to the revisions noted above, the cell array efficiency (CAE – the Array % of total chip area) was change to 56.1% after 2006. Only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery, however, the CAE pull-in enables the production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
SRAM Cell (6-transistor) Area factor ++	**97.5**	**100.7**	**104.1**	**107.8**	**106.7**	**105.7**	**104.8**	**104.1**	**103.4**
Logic Gate (4-transistor) Area factor ++	**279**	**292**	**306**	**320**	**320**	**320**	**320**	**320**	**320**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
SRAM Cell (6-transistor) Area (um2)++	**0.45**	**0.35**	**0.28**	**0.22**	**0.17**	**0.13**	**0.11**	**0.084**	**0.066**
SRAM Cell (6-transistor) Area w/overhead (um2)++	**0.73**	**0.57**	**0.45**	**0.35**	**0.27**	**0.22**	**0.17**	**0.13**	**0.11**
Logic Gate (4-transistor) Area (um2) ++	**1.3**	**1.0**	**0.82**	**0.65**	**0.51**	**0.41**	**0.32**	**0.26**	**0.20**
Logic Gate (4-transistor) Area w/overhead (um2) ++	**2.6**	**2.1**	**1.6**	**1.3**	**1.0**	**0.82**	**0.65**	**0.51**	**0.41**
Transistor density SRAM (Mtransistors/cm^2)	**827**	**1,057**	**1,348**	**1,718**	**2,187**	**2,781**	**3,532**	**4,484**	**5,687**
Transistor density logic (Mtransistors/cm^2)	**154**	**194**	**245**	**309**	**389**	**490**	**617**	**778**	**980**
*Generation at introduction **	**p10c**	**p10c**	**p13c**	**p13c**	**p13c**	**p16c**	**p16c**	**p16c**	**p19c**
Functions per chip at introduction (million transistors [Mtransistors])	**773**	**773**	**1546**	**1546**	**1546**	**3092**	**3092**	**3092**	**6184**
Chip size at introduction (mm^2) ‡	**280**	**222**	**353**	**280**	**222**	**353**	**280**	**222**	**353**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**276**	**348**	**438**	**552**	**696**	**876**	**1104**	**1391**	**1753**
*Generation at production **	**p07c**	**p07c**	**p07c**	**p10c**	**p10c**	**p10c**	**p13c**	**p13c**	**p13c**
Functions per chip at production (million transistors [Mtransistors])	**386**	**386**	**386**	**773**	**773**	**773**	**1546**	**1546**	**1546**
Chip size at production (mm^2) §§	**140**	**111**	**88**	**140**	**111**	**88**	**140**	**111**	**88**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**276**	**348**	**438**	**552**	**696**	**876**	**1104**	**1391**	**1753**

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
SRAM Cell (6-transistor) Area factor ++	**102.8**	**102.2**	**101.7**	**101.3**	**100.9**	**100.5**	**100.1**
Logic Gate (4-transistor) Area factor ++	**320**	**320**	**320**	**320**	**320**	**320**	**320**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
SRAM Cell (6-transistor) Area (um2)++	**0.052**	**0.041**	**0.032**	**0.026**	**0.020**	**0.016**	**0.01**
SRAM Cell (6-transistor) Area w/overhead (um2)++	**0.083**	**0.066**	**0.052**	**0.041**	**0.032**	**0.026**	**0.020**
Logic Gate (4-transistor) Area (um2) ++	**0.16**	**0.13**	**0.10**	**0.081**	**0.064**	**0.051**	**0.040**
Logic Gate (4-transistor) Area w/overhead (um2) ++	**0.32**	**0.26**	**0.20**	**0.16**	**0.13**	**0.10**	**0.08**
Transistor density SRAM (Mtransistors/cm^2)	**7,208**	**9,130**	**11,558**	**14,625**	**18,497**	**23,394**	**29,588**
Transistor density logic (Mtransistors/cm^2)	**1,235**	**1,555**	**1,960**	**2,469**	**3,111**	**3,920**	**4,938**
*Generation at introduction **	**p19c**	**p19c**	**p22c**	**p22c**	**p22c**	**p25c**	**p25c**
Functions per chip at introduction (million transistors [Mtransistors])	**6184**	**6184**	**12368**	**12368**	**12368**	**24736**	**24736**
Chip size at introduction (mm^2) ‡	**280**	**222**	**353**	**280**	**222**	**353**	**280**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**2209**	**2783**	**3506**	**4417**	**5565**	**7012**	**8834**
*Generation at production **	**p16c**	**p16c**	**p16c**	**p19c**	**p19c**	**p19c**	**p22c**
Functions per chip at production (million transistors [Mtransistors])	**3092**	**3092**	**3092**	**6184**	**6184**	**6184**	**12368**
Chip size at production (mm^2) §§	**140**	**111**	**88**	**140**	**111**	**88**	**140**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**2209**	**2783**	**3506**	**4417**	**5565**	**7012**	**8834**

Notes for Tables 1g and 1h:

++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p04c, was introduced in 2002, but not ramped into volume production until 2004; similarly, the p07c, is introduced in 2004, but is targeted for volume production in 2007.*

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/2000) plus Logic (20M transistors in 1 core in year 2000); and the combination of both SRAM and logic transistor functionality doubles every technology cycle. The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2022 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Logic (Low-volume Microprocessor) High-performance ‡									
Generation at Introduction	**p10h**	**p10h**	**p13h**	**p13h**	**p13h**	**p16h**	**p16h**	**p16h**	**p19h**
Functions per chip at introduction (million transistors)	**2212**	**2212**	**4424**	**4424**	**4424**	**8848**	**8848**	**8848**	**17696**
Chip size at introduction (mm^2)	**620**	**492**	**391**	**620**	**492**	**391**	**620**	**492**	**391**
*Generation at production ***	**p07h**	**p07h**	**p07h**	**p10h**	**p10h**	**p10h**	**p13h**	**p13h**	**p13h**
Functions per chip at production (million transistors)	**1106**	**1106**	**1106**	**2212**	**2212**	**2212**	**4424**	**4424**	**4424**
Chip size at production (mm^2) §§	**310**	**246**	**195**	**310**	**246**	**195**	**310**	**246**	**195**
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	**357**	**449**	**566**	**714**	**899**	**1133**	**1427**	**1798**	**2265**
ASIC									
ASIC usable Mtransistors/cm^2 (auto layout)	**357**	**449**	**566**	**714**	**899**	**1133**	**1427**	**1798**	**2265**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	***858***	***858***	***858***	***858***	***858***	***858***	***858***	***858***	***858***
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**3,061**	**3,857**	**4,859**	**6,122**	**7,713**	**9,718**	**12,244**	**15,427**	**19,436**

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Logic (Low-volume Microprocessor) High-performance ‡							
Generation at Introduction	**p19h**	**p19h**	**p22h**	**p22h**	**p22h**	**p25h**	**p25h**
Functions per chip at introduction (million transistors)	**17696**	**17696**	**35391**	**35391**	**35391**	**70782**	**70782**
Chip size at introduction (mm^2)	**620**	**492**	**391**	**620**	**492**	**391**	**620**
*Generation at production ***	**p16h**	**p16h**	**p16h**	**p19h**	**p19h**	**p19h**	**p22h**
Functions per chip at production (million transistors)	**8848**	**8848**	**8848**	**17696**	**17696**	**17696**	**35391**
Chip size at production (mm^2) §§	**310**	**246**	**195**	**310**	**246**	**195**	**310**
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	**2854**	**3596**	**4531**	**5708**	**7192**	**9061**	**11416**
ASIC							
ASIC usable Mtransistors/cm^2 (auto layout)	**2854**	**3596**	**4531**	**5708**	**7192**	**9061**	**11416**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	***858***	***858***	***858***	***858***	***858***	***858***	***1716***
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**24,488**	**30,853**	**38,873**	**48,977**	**61,707**	**77,746**	**195,906**

Notes for Tables 1i and 1j:

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p04c, was introduced in 2002, but not ramped into volume production until 2004; similarly, the p07c, is introduced in 2004, but is targeted for volume production in 2007.*

‡ MPU High-performance Model—High-performance MPU includes Level 2 (L2) on-chip SRAM (2048Kbyte in year 2000) plus Logic (25M transistors in 1 core in year 2000), and the combination of both SRAM and logic transistor functionality doubles every technology cycle. The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2022 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

CHIP-SIZE, LITHOGRAPHIC-FIELD, AND WAFER-SIZE TRENDS

Despite the continuous reduction in feature size of about 30% every two to three years, the chip size of first introductory-level leading-edge memory and logic product demonstrations in technical forums such as the IEEE International Solid State Circuits Conference (ISSCC) have continued to double every six years (an increase of about 12%/year). This increase in chip area has been necessary to accommodate 40%–60% more bits/capacitors/transistors per year in accordance with Moore's Law (historically doubling functions per chip every 1.5–2 years). However, to maintain the historical trend of reducing the leading-edge product cost/function by ~30%/year, it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, maintain or increase wafer and silicon area throughput, and, most of all, increase the number of functionality (transistors, bits, logic gates) and chips available on a wafer.

The increase in the gross number of functions and chips available on a wafer is primarily obtained by reducing the area of the functions and chips by means of a combination of smaller feature size (shrink/scaling) and product/process redesign (compaction). For instance, using the latest ITRS product chip size models, it is forecast that the introduction chip area of a cost-effective product generation [which doubles the inter-generation (generation-to-generation) functionality every two years] must remain as flat as possible. Furthermore, the area must be shrunk at an intra-generation (within a generation) annual reduction rate of 50% (the square of the .7× lithography reduction rate) during every technology cycle period, or faster when additional design-factor-related density improvement is available.

In order for affordable DRAM and Flash memory products to achieve virtually flat intra-generation chip-sizes, they must also maintain a cell area array efficiency ratio of 58–63% of total chip area. Historically, DRAM and Flash memory products have required reduction of cell area design factors (a) (cell area (Ca) in units of minimum-feature size (f) squared; $Ca = af^2$). The PIDS and FEP ITWGs have provided member survey data for the array efficiency targets, the cell area factors, and bits per chip. In addition, detailed challenges and needs for solutions to meet the aggressive cell area goals are documented in the Front End Processes chapter. Due to the importance of tracking/coordinating these new challenges, the DRAM and Flash memory cell area factors, the target cell sizes, and the cell array area percentage of total chip-size line items will continue to be tracked in ORTC Tables 1c, d, e, and f. (also refer to the Glossary for additional details).

Notably, the most recent survey data and publicly available announcements indicate that reduction rate of DRAM cell area factors for the 2007 ITRS models have accelerated, placing the 6 area factor in 2006 (versus 2008 in the 2005 ITRS). The area factor is still expected to remain flat at 6 through the 2020 ITRS horizon. In addition to the 6 factor pull-in, the survey pulled in the 56% array efficiency to begin in 2006. These gains in DRAM cell design efficiency and function density were traded off against a lower targeted production chip size starting point (100mm2 in 2007 versus 140mm2 in 2005) Therefore, the DRAM "Moore's Law" bits per chip targets have been delayed by 1 year, and continue to target 2× every three years in both the near term and long term. The 64 Gbit DRAM product now sits at the ITRS year 2022 horizon (refer to Function Size and Functions per Chip in Figures 8 and 9).

In the updated 2007 ORTC Flash product model, the function bit size is still calculated based upon it's the design factor and the also the critical feature scaling of the uncontacted polysilicon dense lines. The 2007 PIDS Flash survey indicated that the rapid 2-year scaling cycle will continue through 2008, however the single-level-cell physical design factor limit

remains at 4. Therefore, the Flash model function (bit size) area reduction accelerated, and the Flash uncontacted polysilicon half-pitch now leads the DRAM stagger-contacted M1 half-pitch by two years. The Lithography TWG now believes that leading-edge Flash manufacturing technology is driving the most-leading-edge manufacturing, but is still using comparable processing equipment as leading-edge DRAM.

Flash single-level-cell (SLC) bit technology was thus able to drive quickly to a 76 nm uncontacted polysilicon half-pitch and a "4" design factor in 2005; and to continue the scaling reduction to 45nm in 2008, reducing SLC bit size to 0.008 um2, more than one-half the size of a DRAM cell that year (see Figure 8, 2005 ITRS Product Function Size Trends). This continued acceleration of Flash technology will enable the production of a 144 mm^2 8 Gbit SLC product in 2007, when DRAM product is still at 2 Gbit. Furthermore, Flash technology is able to create an electrical doubling of bits (multi-level-cell, or MLC) in the same area, resulting in a virtual doubling of bits per chip to 16 Gbits in the 140 mm^2 affordable first production chip size range. The PIDS Flash survey has also placed a quad-bit MLC beginning 2010 in production.

In the 2001 ITRS the Design ITWG improved the MPU chip size model to update with the latest transistor densities, large on-chip SRAM, and smaller target chip sizes. The Design ITWG added additional detail to the model, including transistor design improvement factors. The original Design ITWG model notes that design improvements occur at a slow rate in SRAM transistors and very little in logic gate transistors. Almost all the "shrink" and density improvement comes from lithography-enabled interconnect half-pitch scaling alone.

The present 2007 ITRS MPU model still "starts" in 2000/180 nm (versus original 1999/180 nm) chip size model is unchanged from the 2001 ITRS, and continues to reflect the additional competitive requirements for affordability and power management by targeting flat chip size trends for both high-performance MPUs (310 mm^2) and cost-performance MPUs (140 mm^2). Due to the MPU two-year-cycle half-pitch "catch-up phase" through the year 2004, the MPU products may be able to maintain flat chip sizes due to lithography improvements alone. However, after 2004, the inter-generation MPU chip size model, which is indexed to the ITRS technology cycles, can remain flat only by slowing the rate of on-chip transistors to double every technology generation. In a 2007 update, the MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends. Refer to Function Size and Functions per Chip in Figures 8 and 9.

Due to the forecasted return to a three-year technology cycle, the present MPU chip-size model slows the Moore's Law rate of on-chip transistors to 2× every three years. In order to maintain a flat chip size target and also return to the historical doubling every two years of on-chip functionality (transistors), MPU chip and process designers must add additional design/process improvements to the fundamental lithography-based scaling trends. The new target metrics of the MPU model are summarized in Tables 1g, h, i, and j.

To improve productivity, it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is a key productivity driver and is determined by the field size of the lithographic tool and the size and aspect ratio of the chips being printed on the wafer. In the past, lithography exposure field sizes doubled every other technology to meet the demand for increasing maximum introduction-level chip sizes. The result was the achievement of very large step-and-scan fields (26×33 = 858 mm^2).

However, the Lithography ITWG indicates that maintaining the large field size under continued reduction of exposure features is increasing costs dramatically. Therefore, the Lithography ITWG is dependent upon the individual memory and logic product chip size models to drive the requirements for both the absolute maximum field size and also the more typical affordable field size ranges.

DRAM chip sizes have historically been the most appropriate driver of both the most difficult half-pitch exposures and also the affordable lithography field size range. In the 2007 ITRS chip-size model for DRAMs, the introduction-level chip size is targeted to be smaller than a 704 mm^2 lithography field size, fitting at least one introduction-level chip size within that field size. The latest 2007 ITRS production-level DRAM chip size model (less than 100 mm^2 flat target) fits five die within a 572 mm^2 field.

The combination of technology generation scaling and cell design improvements (A-factor reduction) accomplishes that goal, while also maintaining a goal of doubling on-chip bits every two years. However, as mentioned in the product chip size model discussions above, the slowing of DRAM design improvements, and the new 100mm2 affordable production chip size target, causes a requirement to add fewer on-chip bits to stay under the affordable chip size and lithography field size. This is accomplished in the present DRAM model by delaying the production bits/chip generations by 1 year, and slowing the Moore's Law bits/chip rate to 2×/ three years, as required. The data targets for the DRAM model are included

in Tables 1c, d, e, and f. The new Flash production chip size model is also included in those tables, and still targets the Flash maximum affordable chip size at 140 mm^2.

The absolute maximum lithography field size is driven by the early introduction level chip sizes of high-performance MPUs and ASICs, which approach the maximum practical field size available from the Lithography TWG ($26 \times 33 = 858$ mm^2). It is anticipated that future mask magnification levels as high as 8× may reduce the maximum field size to one-fourth the present 858 mm^2, reducing the maximum available area to less than 214 mm^2. The details surrounding the limitations of maximum field size and the mask magnification issue will be developed by the Lithography TWG in their chapter. The maximum Lithography field size is shown in Tables 2a and b.

The 2007 ITRS DRAM, MPU and Flash models depend upon achieving the aggressive DRAM, MPU, and Flash design and process improvement targets. If those targets slip, then pressure will increase to print chip sizes larger than the present roadmap, or further slow the rate of "Moore's-Law" on-chip functionality. Either of these consequences will result in a negative impact upon cost-per-function reduction rates—the classical measure of our industry's productivity-improvement and competitiveness.

With increasing cost-reduction pressures, the need for the 300 mm productivity boost will also increase in urgency, especially for leading-edge manufacturers, but the poor economy has created financial challenges and limited capital investment. The maximum substrate diameter in Tables 2a and b (and in additional detail in the FEP chapter) is consistent with the ramp of 300 mm capacity beginning 2001. Also, the first manufacturing capability for the next 1.5× wafer size conversion to 450 mm diameter is still not anticipated to be required until 2012 in the present Roadmap. However, should the other productivity-improvement drivers (lithography and design/process improvements) fail to stay on schedule, there would be a need to accelerate the use of increased wafer diameter, or an equivalent processing platform, as a productivity improvement.

The effects of future technology acceleration/deceleration and the timing of the next wafer generation conversion require the development and application of comprehensive long-range factory productivity and industry economic models. Such industry economic modeling (IEM) work is being sponsored and carried out jointly by Semiconductor Equipment and Materials International (SEMI) and SEMATECH. Most certainly, pre-competitive cooperation between the semiconductor supplier and manufacturer companies will be required to define the future technical and economic needs and to identify appropriate funding mechanisms for the required research and development.

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Lithography Field Size									
Maximum Lithography Field Size—area (mm^2)	**858**	**858**	**858**	**858**	**858**	**858**	**858**	**858**	**858**
Maximum Lithography Field Size—length (mm)	**33**	**33**	**33**	**33**	**33**	**33**	**33**	**33**	**33**
Maximum Lithography Field Size—width (mm)	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)									
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300 or 450**	**300 or 450**	**300 or 450**	**300 or 450**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
Lithography Field Size							
Maximum Lithography Field Size—area (mm^2)	**858**	**858**	**858**	**858**	**858**	**858**	**858**
Maximum Lithography Field Size—length (mm)	**33**	**33**	**33**	**33**	**33**	**33**	**33**
Maximum Lithography Field Size—width (mm)	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**450**	**450**	**450**	**450**	**450**	**450**	**450**

PERFORMANCE OF PACKAGED CHIPS

NUMBER OF PADS AND PINS / PAD PITCH, COST PER PIN, FREQUENCY

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. (Refer to Tables 3a and b).

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. Based upon chip pad-count numbers supplied by the Test ITWG, logic products (MPUs and high-performance ASICs) both approach 4–6K pads over the ITRS period. The MPU products are forecast to increase the total number of pads through this period by nearly 50%, and the ASICs double the maximum number of pads per chip. The two product types also differ significantly in the ratio of power/ground pads. The MPU product pad counts typically have 1:3 signal I/O pads and 2:3 power and ground pads, or two power/ground pads for every signal I/O pad. Unlike MPUs, high-performance ASIC product pad counts typically include one power/ground pad for each signal I/O pad.

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Number of Chip I/Os (Number of Total Chip Pads)—Maximum									
Total pads—MPU unchanged	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**
Signal I/O—MPU (% of total pads)	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**
Power and ground pads—MPU (% of total pads)	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**
IS: Total pads—ASIC High Performance unchanged	**4,400**	**4,400**	**4,600**	**4,800**	**4,800**	**5,000**	**5,400**	**5,400**	**5,600**
Signal I/O pads—ASIC high-performance (% of total pads)	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**
Power and ground pads—ASIC high-performance (% of total pads)	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**
Number of Total Package Pins—Maximum [1]									
Microprocessor/controller, cost-performance	**600–2140**	**600–2400**	**660–2801**	**660–2783**	**720-3061**	**720–3367**	**800–3704**	**800-4075**	**880–4482**
Microprocessor/controller, high-performance	**4000**	**4400**	**4620**	**4851**	**5094**	**5348**	**5616**	**5896**	**6191**
ASIC (high-performance)	**4000**	**4400**	**4620**	**4851**	**5094**	**5348**	**5616**	**5896**	**6191**

Notes for Tables 3a and 3b:

[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by printed wiring board (PWB) technology and system cost. The highest pin count applications will as a result use larger pitches and larger package sizes. The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4.

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
Number of Chip I/Os (Number of Total Chip Pads)—Maximum							
Total pads—MPU unchanged	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**
Signal I/O—MPU (% of total pads)	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**
Power and ground pads—MPU (% of total pads)	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**
IS: Total pads—ASIC High Performance unchanged	**6,000**	**6,000**	**6,200**	**6,200**	**6,200**	**6,840**	**6,840**
Signal I/O pads—ASIC high-performance (% of total pads)	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**
Power and ground pads—ASIC high-performance (% of total pads)	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**
Number of Total Package Pins—Maximum [1]							
Microprocessor/controller, cost-performance	**880–4930**	**960-5423**	**960–5966**	**1050-6562**	**1050 - 7218**	**1155-7940**	**1155-8337**
Microprocessor/controller, high-performance	**6501**	**6826**	**7167**	**7525**	**7902**	**8297**	**8712**
ASIC (high-performance)	**6501**	**6826**	**7167**	**7525**	**7902**	**8297**	**8712**

Package pin count (Tables 3a and 3b) and cost-per-pin (Tables 4a and 4b), provided by the Assembly and Packaging ITWG, point out challenges to future manufacturing economics. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will continue to grow, while the cost/pin decreases. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions, because the overall average cost of packaging will increase annually.

In the very competitive consumer electronics product environment (which is a focus end-product segment for characterizing Design and System-Driver Chapter Grand Challenges and Potential Solutions), prices for high-volume, high-tech products such as PCs and cell phones tend to remain flat or even decrease. These same high-tech products typically also deliver twice the performance every two years. This is the end-use market environment of the leading-edge semiconductor manufacturer, and it is the fundamental economic driver behind the ITRS economic requirement to reduce cost per function (bits, transistors) at an annual 30% or faster rate (2× functionality/chip at flat price every two years = 29%/year).

If future semiconductor component products must be targeted to maintain constant or decreasing prices and the average number of pins per unit increases while the average cost per pin decreases , then: the average packaging share of total product cost will continue to increase over the 15-year roadmap period; and

3. the ultimate result will be greatly reduced gross profit margins and limited ability to invest in R&D and factory capacity.

This conclusion is one of the drivers behind the industry trends to reduce the overall system pin requirements by combining functionality into systems-on-chip (SOC) and through the use of multi-chip modules (System-in-Package, i.e., SiP), bumped chip-on-board (COB), and other creative solutions.

In addition to the need to increase functionality while exponentially decreasing cost per function, there is also a market demand for higher-performance, cost-effective products. Just as Moore's Law predicts that functions-per-chip will double every 1.5–2 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. In the case of MPUs, processor instructions/second have also historically doubled every 1.5–2 years. However, in the latest 2007 ITRS, historical and forecast trends are suggesting a significant slowing in the rate of increase of on-chip frequency, to approximately only 8% growth per year or less. Performance increases accomplished historically by geometrical scaling (refer to Glossary) are now being provided through architecture and software improvements that enable the continued delivery of SOC, SIP, and system-level performance to customers while keeping power management under control.

For MPU products, increased processing power, measured in millions of instructions per second (MIPs), is accomplished through a combination of "raw technology performance" (clock frequency) multiplied by "architectural performance" (instructions per clock cycle). The need for a progressively higher operational performance will continue to demand the development of novel process, design, and packaging techniques.

These considerations are reflected in Tables 4c and 4d, which include line items contributed by the Design TWG to forecast the maximum on- trends. The highest frequency obtainable in each product generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between this "local" frequency and the frequency of signals traveling across the chip increases due to degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package. To optimize signal and power distribution across the chip, it is expected that the number of layers of interconnect will continue to increase. As size downscaling of interconnect also continues, wider use of copper (low resistivity) and various inter-metal insulating materials of progressively lower dielectric constant (κ~2–3) will be adopted in the chip fabrication process. Multiplexing techniques will also be used to increase the chip-to-board operating frequency (off-chip).

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Chip Pad Pitch (micron)									
Pad pitch—ball bond [no update - deleted by A&P]	**30**	**30**	**25**	**25**	**25**	**20**	**20**	**20**	**20**
Pad pitch—wedge bond	**25**	**25**	**25**	**25**	**25**	**25**	**25**	**25**	**25**
Pad Pitch—area array flip-chip (cost-performance, high-performance)	**130**	**130**	**120**	**120**	**120**	**110**	**110**	**100**	**100**
Pad Pitch—2-row staggered-pitch (micron)	**45**	**45**	**40**	**40**	**35**	**35**	**35**	**35**	**35**
Pad Pitch—Three-tier-pitch pitch (micron)	**50**	**50**	**45**	**45**	**40**	**40**	**35**	**35**	**35**
Cost-Per-Pin									
Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly – Cost-performance) — minimum–maximum	**.69-1.19**	**.66-1.13**	**.63-1.70**	**.60-1.20**	**.57-.97**	**.54-.92**	**.51-.87**	**.48 - .83**	**.46 - .79**
Package cost (cents/pin) (Low-cost, hand-held and memory) — minimum–maximum	**.27-.50**	**.25-.48**	**.24-.46**	**.23-.44**	**.22-.42**	**.21-.40**	**.20-.38**	**.20-.36**	**.20 - .34**

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Chip Pad Pitch (micron)							
Pad pitch—ball bond [no update - deleted by A&P]	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Pad pitch—wedge bond	**25**	**25**	**25**	**25**	**25**	**25**	**25**
Pad Pitch—area array flip-chip (cost-performance, high-performance)	**95**	**95**	**90**	**90**	**85**	**85**	**80**
Pad Pitch—2-row staggered-pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Pad Pitch—Three-tier-pitch pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Cost-Per-Pin							
Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly – Cost-performance) — minimum–maximum	**.44 - .75**	**.42 - .71**	**.39 - .68**	**.37 - .64**	**.35 - .61**	**.33-.58**	**0.32-0.55**

Package cost (cents/pin) (Low-cost, hand-held and memory) — minimum–maximum	.20-.32	.20-.30	.20-.29	.20-.27	.20-.26	.19-.25	.19-.25

Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	36	32	28	25
Flash ½ Pitch (nm) (un-contacted Poly)(f)	54	45	40	36	32	28	25	22	20
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	68	59	52	45	40	36	32	28	25
MPU Physical Gate Length (nm)	25	23	20	18	16	14	13	11	10
Chip Frequency (MHz)									
On-chip local clock [1]	**4.700**	**5.063**	**5.454**	**5.875**	**6.329**	**6.817**	**7.344**	**7.911**	**8.522**
Maximum number wiring levels [3] **[**]**	**11**	**12**	**12**	**12**	**12**	**12**	**13**	**13**	**13**

Table 4d Performance and Package Chips: Frequency On-chip Wiring Levels—Long-term Years

Year of Production	2016	2017	2018	2019	2020	2021	2022
DRAM ½ Pitch (nm) (contacted)	22	20	18	16	14	13	11
Flash ½ Pitch (nm) (un-contacted Poly)(f)	18	16	14	13	11	10	9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	22	20	18	16	14	13	11
MPU Physical Gate Length (nm)	9	8	7	6	6	5	4
Chip Frequency (MHz)							
On-chip local clock [1]	**9.180**	**9.889**	**10.652**	**11.475**	**12.361**	**13.315**	**14.343**
Maximum number wiring levels [3] **[**]**	**13**	**14**	**14**	**14**	**14**	**15**	**15**

*[**] [Note ** : The Interconnect TWG has deleted their "optional levels" from table 80a&b, therefore the ORTC "Maximum number wiring levels - maximum" line is deleted; also the "Maximum number wiring levels - minimum" is now just "Maximum number of wiring levels."*

Note for Tables 4c and 4d:

[1] The on-chip frequency is based on the fundamental transistor delay (defined by the PIDS TWG), and an assumed maximum number of 12 inverter delays beginning 2007; after 2007, the PIDS model fundamental reduction rate of ~ -14.7% for the transistor delay results in an individual transistor frequency performance rate increase of ~17.2% per year growth. In the 2005 roadmap, the trend of the on-chip frequency was also increased at the same rate of the maximum transistor performance through 2022. Although the 17% transistor performance trend target is continued in the PIDS TWG outlook, the Design TWG has revised the long-range on-chip frequency trend to be only about 8% growth rate per year. This is to reflect recent on-chip frequency slowing trends and anticipated speed-power design tradeoffs to manage a maximum 200 watts/chip affordable power management tradeoff.

[2] The off-chip frequency, is defined by the Assembly and Packaging (A&P) model, and is available in the A&P chapter.

[3] The maximum number of interconnect wiring levels includes the optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

ELECTRICAL DEFECT DENSITY

The latest targets for electrical defect density of DRAM, MPU, and ASIC (necessary to achieve 83–89.5 % chip yield in the year of volume production) are shown in Tables 5a and b. The allowable number of defects is calculated by taking into account the different chip sizes based on the latest chip size model forecasts, as reported in Table 1 for DRAM and microprocessors. In addition, the data in the table are now reported only at the production-level of the product life-cycle. Other defect densities may be calculated at different chip sizes at the same technology by using the formula found in the Yield Enhancement chapter. The approximate number of masks for logic devices is included as an indicator of the ever-increasing process complexity.

Table 5a Electrical Defects—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
DRAM Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater §	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**
MPU Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater §§	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**
# Mask Levels—MPU	**33**	**35**	**35**	**35**	**35**	**35**	**37**	**37**	**37**
# Mask Levels—DRAM	**24**	**24**	**26**	**26**	**26**	**26**	**26**	**26**	**26**

Table 5b Electrical Defects—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
DRAM Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater §	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**
MPU Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater §§	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**
# Mask Levels—MPU	**37**	**39**	**39**	**39**	**39**	**39**	**39**
# Mask Levels—DRAM	**26**	**26**	**26**	**26**	**26**	**26**	**26**

Notes for Tables 5a and 5b:

D_0 — defect density

§ DRAM Model—cell area factor (design/process improvement) targets are as follows:

1999–2006/8×: 2006-2022/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the last model 2005 ITRS timeframe refer to Figures 8 and 9 for bit size and bits/chip trends:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2022 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

POWER SUPPLY AND POWER DISSIPATION

The reduction of power supply voltage is driven by several factors—reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. As seen in Tables 6a and b, the value of the power supply voltage is now given as a range.

Selection of a specific V_{dd} value continues to be a part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each product generation. Values of V_{dd} as low as 0.5 volts are not expected to be achieved by high-performance processors until beyond 2022. . The lowest V_{dd} target is still 0.5V in 2016 for the low operating power applications, but is targeted to drop to 0.45 volts in 2021.

Maximum power trends (e.g., for MPUs) are presented in three categories—1) high-performance desktop applications, for which a heat sink on the package is permitted; 2) cost-performance, where economical power management solutions of the highest performance are most important; and 3) portable battery operations (now designated as the "Harsh" application category by the Assembly and Packaging TWG). In all cases, total power consumption continues to increase, despite the use of a lower supply voltage. The increased power consumption is driven by higher chip operating frequencies (significantly reduced in the 2007 roadmap from 17% CAGR to 8% CAGR), the higher interconnect overall capacitance and resistance, and the increasing gate leakage of exponentially growing and scaled on-chip transistors.

Table 6a Power Supply and Power Dissipation—Near-term Years

[1] Power will be limited more by system level cooling and test constraints than packaging

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Power Supply Voltage (V)									
Vdd (high-performance)	**1.1**	**1.0**	**1.0**	**1.0**	**0.95**	**0.90**	**0.90**	**0.90**	**0.80**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.80**	**0.80**	**0.80**	**0.70**	**0.70**	**0.70**	**0.60**	**0.60**	**0.60**
Allowable Maximum Power [1]									
High-performance with heatsink (W)	**189**	**198**	**198**	**198**	**198**	**198**	**198**	**198**	**198**
Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	**310**	**310**	**310**	**310**	**310**	**310**	**310**	**310**	**310**
Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	**0.61**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**
Cost-performance (W)	**104**	**111**	**116**	**119**	**119**	**125**	**137**	**137**	**137**
Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	**0.74**	**0.79**	**0.83**	**0.85**	**0.85**	**0.89**	**0.98**	**0.98**	**0.98**
Battery (W)—(low-cost/hand-held)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Table 6b Power Supply and Power Dissipation—Long-term Years

[1] Power will be limited more by system level cooling and test constraints than packaging

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Power Supply Voltage (V)							
Vdd (high-performance)	**0.80**	**0.70**	**0.70**	**0.70**	**0.65**	**0.65**	**0.65**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.45**	**0.45**
Allowable Maximum Power [1]							
High-performance with heatsink (W)	**198**	**198**	**198**	**198**	**198**	**198**	**198**
Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	**310**	**310**	**310**	**310**	**310**	**310**	**310**
Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**
Cost-performance (W)	**151**	**151**	**151**	**151**	**151**	**151**	**151**
Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	**1.08**	**1.08**	**1.08**	**1.08**	**1.08**	**1.08**	**1.08**
Battery (W)—(low-cost/hand-held)	**3**	**3**	**3**	**3**	**3**	**3**	**3**

COST

Tables 7a and 7b are dedicated to cost trends. The historical ability to reduce the leading-edge product manufacturing cost per function by an average 29% each year has represented one of the unique features of the semiconductor industry and is a direct consequence of the market pressure to continue to deliver twice the functionality on-chip every 1.5–2 years in an environment of constant or reducing prices. In support of this market cost reduction mandate, a continuously increasing amount of investment is needed for R&D and manufacturing capital. Even on a per-factory basis, the capital cost of manufacturing continues to escalate. Yet, the semiconductor industry has historically delivered two times as many functions per chip every 1.5–2 years with an approximately constant cost per cm2 of silicon. This technological and economic performance is the fundamental engine behind the growth of the semiconductor industry.

However, the customers in today's challenging economic and competitive market environment continue to resist even moderate increases in per unit cost, maintaining the pressure upon the semiconductor industry to slow the rate of doubling functions per chip (Moore's Law) in order to keep chip and unit costs under control. The semiconductor manufacturers had to seek a new model to deliver the same cost-per-function reduction requirements that have fueled industry growth. Consequently, the 1999 ITRS proposed a new model for achieving the required reduction: provide the customer twice the functionality every two years at constant cost targets. The 2001 and 2003, 2005, and now the 2007 ITRS models *all continue to use that model*, which results in 29% cost reduction of a function (bit, transistor, etc.). That rate of function cost reduction was achieved historically (prior to 1999) by delivering four times the functionality per chip every three years at 1.4× increase in cost per unit.

The 2007 ITRS DRAM and MPU cost models continue to use the need for that 29% cost-per-function productivity reduction rate as an economic driver of the industry. Therefore, that core cost-per-function trend has been used to set the INTRA-generation trends for the affordable cost/bit and cost/transistor for DRAM and microprocessors, respectively. Extrapolation of historical trends would indicate an "at introduction" affordable cost/bit of 5.3 microcents for 8 Gbit DRAMs in 2003. In addition, the historical trends indicate that, within a DRAM generation, a 45%/year reduction in cost/bit should be expected.[2] A corresponding analysis conducted from published data for microprocessors yields similar

[2] *McClean, William J., ed. Mid-Term 1994: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1994.*
McClean, William J., ed. Mid-Term 1995: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1995.

results.[3] Therefore, the 29%/year target for reduction in affordable cost/transistor from generation to generation is also being used in the MPU model, along with the 45%/year reduction rate within the same generation.

The 2007 ITRS retains the original 2001 MPU chip size model. The Design ITWG updated the MPU model in the 2001 ITRS, based upon available data. At that time, the data indicated that logic transistor size is improving only at the rate of the lithography (0.7× linear, 0.5× area reduction every technology cycle). Therefore, in order to keep the MPU chip sizes flat, the number of transistors can be doubled only every technology cycle. The technology cycle rate is projected to be on a 2.5-year cycle from 180nm/2001 through 45nm/2010, and return to a three-year cycle after 2010. Therefore the transistors per MPU chip can double only every three years after 2004, unless increased chip size is allowed for specific applications which have markets that can afford the higher costs.

DRAM memory bit cell design improvements accelerated slightly, as reflected in the 2007 ITRS DRAM Chip Size Model targets. The “6” design factor, a 25% improvement over the “8” factor, was actually implemented in 2006, (versus 2008 in 2005 roadmap). However, the “5” design factor target, is still not anticipated, slowing the long-range cost-reduction productivity. However, the latest PIDS TWG survey of DRAM manufacturers has indicated that the target for the cell array efficiency percentage achieved 56% after 2006 (versus 2008 in 2005 roadmap). The combination of these recent model changes, along with the new goal of a more affordable starting production chip size (less than 100mm2 versus previous 140mm2) has delayed the bits/chip increase rate of DRAM by one year, and continued the rate of bits per chip at 2×/3 years. These DRAM model changes have pushed the 64 Gbit generation (introduction in 2013) to 2022 for production and moved the 128 Gbit DRAM (introduction 2016) beyond the present 2022 ITRS horizon. .

To compensate for slowing DRAM and MPU functions-per-chip, there will be increasing pressure to find alternative productivity enhancements from the “equivalent” productivity scaling benefits of chip, package, board, and system-level architecture and designs.

Even though the rate of increase of on-chip functionality could slow in the future, the amount of functions/chip is still growing exponentially, though at a slower rate. As the number of functions/chip continues to increase, it becomes increasingly difficult and, therefore, costly to test the final products. This issue is reflected in the escalating cost of testers. The number of tested pins (Tables 4a and 4b) is also increasing, which adds to the cost of the tester as well as the associated material and custom test fixtures that increase the total cost of ownership. Therefore, there will be an ongoing need for accelerated implementation of built-in-self-test and design-for-testability and design-for-manufacturability techniques within the time frame of the 2007 ITRS. Further discussion is detailed in the Test chapter.

Table 7a Cost—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Affordable Cost per Function ++									
DRAM cost/bit at (packaged microcents) at samples/introduction	**2.6**	**1.9**	**1.3**	**0.9**	**0.7**	**0.5**	**0.3**	**0.2**	**0.2**
DRAM cost/bit at (packaged microcents) at production §	**0.96**	**0.68**	**0.48**	**0.34**	**0.24**	**0.17**	**0.12**	**0.08**	**0.06**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**22.0**	**15.6**	**11.0**	**7.8**	**5.5**	**3.9**	**2.8**	**1.9**	**1.4**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**13.3**	**9.4**	**6.7**	**4.7**	**3.3**	**2.4**	**1.7**	**1.2**	**0.83**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**12.2**	**8.6**	**6.1**	**4.3**	**3.0**	**2.2**	**1.5**	**1.1**	**0.76**

[3] *a) Dataquest Incorporated. x86 Market: Detailed Forecast, Assumptions, and Trends. MCRO–WW–MT–9501. San Jose: Dataquest Incorporated, January 16, 1995.*
b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. “The Silicon Age? It's Just Dawning,” Table 1. Business Week, December 9, 1996, 148–152.

Table 7b Cost—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**0.1**	**0.1**	**0.1**	**0.0**	**0.0**	**0.0**	**0.0**
DRAM cost/bit at (packaged microcents) at production §	**0.04**	**0.03**	**0.02**	**0.01**	**0.01**	**0.01**	**0.01**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**0.97**	**0.69**	**0.49**	**0.34**	**0.24**	**0.17**	**0.12**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**0.59**	**0.42**	**0.29**	**0.21**	**0.15**	**0.10**	**0.07**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**0.54**	**0.38**	**0.27**	**0.19**	**0.13**	**0.10**	**0.07**

Notes for Tables 7a and 7b:

++ Affordable packaged unit cost per function based upon average selling prices (ASPs) available from various analyst reports less gross profit margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—cell area factor (design/process improvement) targets are as follows:

1999–2006/8×: 2006-2022/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the last model 2005 ITRS timeframe refer to Figures 8 and 9 for bit size and bits/chip trends:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the latest DRAM consensus model changes for the 2007 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM product are delayed an additional year and now remains "flat" at less than 93 mm^2, about one third smaller than the MPU model. However, with the pull-in of the 6f^2 "cell area factor" , the flat-chip-size model target still requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c, 1d).

In addition to the revisions noted above, the cell array efficiency (CAE – the Array % of total chip area) was change to 56.1% after 2006. Only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery, however, the CAE pull-in enables the production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2007 ITRS, the MPU model still includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target. . The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.

Refer to the Glossary for definitions.

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

2007 ITRS NEW DEFINITION ADDITION FOR "MORE MOORE" AND "MORE THAN MOORE" CONCEPTS

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

SCALING ("MORE MOORE")

a. *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.

b. *Equivalent Scaling* which occurs in conjunction with, and also enables, continued Geometrical Scaling, refers to 3-dimensional device structure ("Design Factor") Improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

FUNCTIONAL DIVERSIFICATION ("MORE THAN MOORE")

Functional Diversification refers to the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (*e.g.,* RF communication, power control, passive components, sensors, actuators) *to migrate from the system board-level* into a particular package-level (SiP) or chip-level (SoC) potential solution.

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets. MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore's Law, there is a historically-based "corollary" to the "law," which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the

cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the 2005 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A Flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1 Mbytes/2001). Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71x/cycle period) generation.

High-performance MPU[4]—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25 Mt cores in 2002) with a large (example 4 Mbyte/2002) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip had increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is still required due to the new consensus 2007 ITRS forecast of cell-area-factor improvement to 6 by 2006, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the 2007 ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The 2003 ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology generation processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM

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[4] *Note: The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.*

products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology generation, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 2 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1 Gb/production, 4 G/introduction, plus 512 Mb/256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2003 ITRS, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.37e-6 mm^2/bit = 397 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half the size of an SLC product cell size and will also have a "virtual area factor" that is half of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology generation. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology generation. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology generation, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first production-qualified development manufacturing facilities.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.